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Five-level NPC-VSI Capacitor Voltage Balancing Using a Novel Clamping Bridge

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Abstract- A serious constraint in multilevel inverters is the capacitor voltage-balancing problem. The unbalance of the different DC voltage sources of the five-level Neutral Point Clamping Voltage Source Inverter (NPC-VSI) constituted the major limitation for the use of this power converter. To remedy to this problem, a new control solution to compensate the unbalanced DC voltages for the five-level NPC VSI is presented. It provides a fast and flexible control of the inverter capacitor voltages, leads to a simpler implementation, and present high equalization efficiency. Simulation results show the effectiveness of our methods.

Keywords- Clamping bridge, five-level , NPC VSI, Lyapunov function, Sliding mode control.

I. INTRODUCTION

In 1980, early interest in multilevel power conversion technology was triggered by the work of Nabae, who introduced the neutral-point-clamped (NPC) inverter topology [1]. It was immediately realized that this new converter had many advantages over the more conventional two-level inverter. Subsequently, the concept of the three-level converter was extended further and some new multilevel topologies were proposed.

An alternative to the diode-clamped converter, the flying capacitor topology does not have issues with clamping diodes. First proposed in 1992 [2], this approach has the advantage of a larger number of redundant switching states, which allows more freedom in balancing the clamping capacitors' voltages. The main disadvantage is the potential for parasitic resonance between the decoupling capacitors; this is made even worse by the high number of capacitors, which complicates packaging for small inductance. In addition, there are issues with voltage redistribution in the case of voltage surges. Nevertheless, the flying capacitor topology seems very promising.

The multilevel configuration with cascaded H-bridge inverters presents another alternative in the design of multilevel converters [3]. A primary advantage of this topology is that it provides the flexibility to increase the number of levels without introducing complexity into the power stage. Also, this topology requires the same number of primary switches as the diode-clamped topology, but does not require the clamping diode.

However, this configuration uses multiple dedicated DC-busses and often a complicated and expensive line transformer, which makes this a rather expensive solution. In addition, bi directional operation is somewhat difficult (although not impossible) to achieve.

Perhaps the most important improvement in cascaded converter topologies is the hybrid multilevel topology [4]. The main strength of this approach is its combination of the high voltage capacity of the relatively slow GTO devices with the high switching frequency of the lower voltage capacity IGBT devices. At the same time, the different voltage levels of the IGBT and GTO bridges create an additional voltage level without any additional complexity.

One important problem associated with the NPC inverter is its Neutral Point (NP) variation [1]. The DC link NP potential can significantly fluctuate or continuously drift to unacceptable levels due to non uniform switching device or DC link capacitor characteristics or fluctuation because of the irregular and unpredictable charging and discharging in each capacitor [5-7].

Some solutions have been proposed, which are based on redundant switching configurations [1] [8-15] or on the addition of zero-sequence voltage components to the output voltage [9].

Unfortunately, these methods modify the output voltage waveform. As the number of inverter-levels increases, the problem of capacitor balancing becomes more complex and the solution very drastic.

The unbalance DC voltage problem can also be solved by separate DC sources [6] or by adding electronic circuitry. In [16-18], clamping bridges based on transistors and resistors are proposed as a solution to this problem.

This paper deals introduces a new clamping bridge for the DC capacitor voltage equalisation has been proposed to DC-link capacitors voltages fluctuations in an NPC VSI that permits to achieve a correct capacitors voltages sharing, when conventional balancing methods compensate fail. The organization of this paper is as follows. Section 2 develops the mathematical modelling of the DC-AC converter five-level NPC-VSI and its Pulse Width Modulation control strategy (PWM) using four bipolar carriers. The control of the two-level PWM current rectifier by Lyapunov function using feedback loops to regulate the average value of DC voltages and the network currents are discussed in section 3. Therefore, a clamping bridge control is introduced to improve the performance of voltage balance strategy in section 4. Finally, in the section 5, simulations will be implemented to present a study of the phenomenon, to demonstrate the proposed method and to report the effectiveness of this solution.

II. FIVE-LEVEL CASCADE

We firstly propose a knowledge model of the three-phase five-level NPC-VSI inverter and develop a PWM strategy to control it (four bipolar carriers). The global scheme of the cascade is given on the Fig 1.

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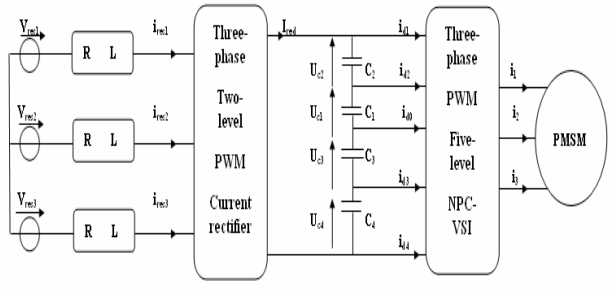

Fig.1: Structure of the cascade proposed

A. Five-level NPC-VSI modelling

The general structure of the three-phase five-level NPC voltage source inverter is shown on the figure 2. It is composed by 24 pairs transistor-diode. Every leg of this inverter includes eight pairs, four on the upper half leg and four on the lower one.

The optimal control law is given below:

$$\begin{cases} B_{k1} = \overline{B_{k5}} \\ B_{k2} = \overline{B_{k4}} \\ B_{k3} = \overline{B_{k6}} \\ B_{k7} = B_{k1}.B_{k2}.\overline{B_{k3}} \\ B_{k8} = B_{k4}.B_{k5}.\overline{B_{k6}} \end{cases} \quad (1)$$

B_{ks} is the control signal of TD_{ks}. TD_{ks} represent every pair transistor-diode by one bi-directional switch.

The voltage of the three-phase A, B, C relatively to the middle point M and using the half leg connection functions F_{kM}^{b} are given by V_{XM} with x = point A, B or C and k=1,2,3.

$$V_{XM} = [F_{k1}^{b}.(U_{c1} + U_{c2}) + F_{k7}.(U_{c1})] - [F_{k0}^{b}.(U_{c3} + U_{c4}) + F_{k8}.(U_{c3})] \quad (2)$$

The input currents of the three-phase five-level inverter using the load currents are given by the following relations:

$$\begin{cases} i_{d1} = F_{11}^{b}.i_1 + F_{21}^{b}.i_2 + F_{31}^{b}.i_3 \\ i_{d2} = F_{11}^{b'}.i_1 + F_{21}^{b'}.i_2 + F_{31}^{b'}.i_3 \\ i_{d3} = F_{10}^{b'}.i_1 + F_{20}^{b'}.i_2 + F_{30}^{b'}.i_3 \\ i_{d4} = F_{10}^{b}.i_1 + F_{20}^{b}.i_2 + F_{30}^{b}.i_3 \\ i_{d0} = i_1 + i_2 + i_3 - i_{d1} - i_{d2} - i_{d3} - i_{d4} \end{cases} \quad (3)$$

B. Control strategy of the inverter

For a five-level inverter, four carrier waves and three modulation signals are used. the modulation waves are compared with the triangular carrier waves and at the intersection points the switching decisions are made for the associated switches.

Pulse Width Modulation (PWM) of multilevel converters is typically an extension of two-level methods. The most common types of multilevel voltage-source PWM are sine-triangle modulation and space-vector modulation (SVM). Multilevel sine-triangle modulation relies on defining a number of triangle waveforms and switching rules for the intersection of these waveforms with a commanded voltage waveform [13–14]. This method is fairly straightforward and insightful for description of multilevel systems.

This strategy uses four bipolar carriers (U_{p1} , U_{p2} , U_{p3}, U_{p4}). It is characterised by two parameters **m** the index modulation and **r** the modulation rate. The algorithm of this strategy can be summarised as follows:

Step 1: Determination of the intermediate voltages

$$\begin{aligned} &\text{If } V_{refk} > U_{p1} \text{ then } V_{XM1} = +U_c \\ &\text{If } V_{refk} < U_{p1} \text{ then } V_{XM1} = 0 \\ &\text{If } V_{refk} > U_{p2} \text{ then } V_{XM2} = +2U_c \\ &\text{If } V_{refk} < U_{p2} \text{ then } V_{XM2} = +U_c \\ &\text{If } V_{refk} > U_{p3} \text{ then } V_{XM3} = 0 \\ &\text{If } V_{refk} < U_{p3} \text{ then } V_{XM3} = -U_c \\ &\text{If } V_{refk} > U_{p4} \text{ then } V_{XM4} = -U_c \\ &\text{If } V_{refk} < U_{p4} \text{ then } V_{XM4} = -2U_c \end{aligned} \quad (4)$$

Step 2: Determination of the output voltage (X=A, B,C)

$$V_{XM} = V_{XM1} + V_{XM2} + V_{XM3} + V_{XM4} \quad (5)$$

III. TWO-LEVEL PWM CURRENT RECTIFIER

The control of the two-level PWM current rectifier by Lyapunov Function using feedback loops to regulate the output DC voltage and the network currents are given.

The general structure of the two-level PWM current rectifier is given on the Fig 3.

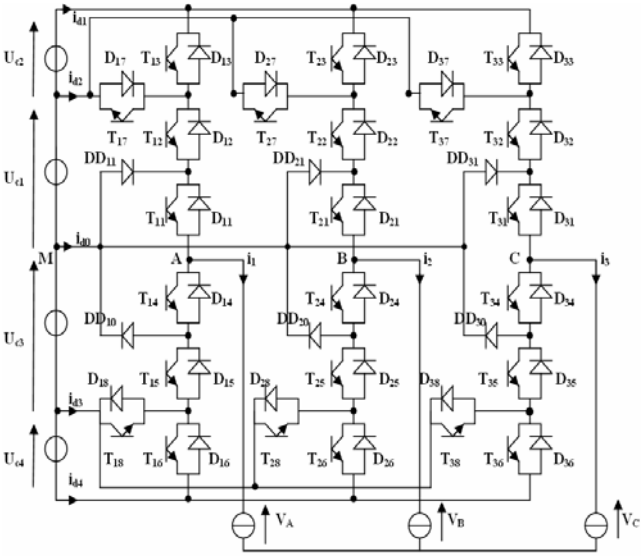

Fig.2: General structure of the three-phase five-level NPC VSI.

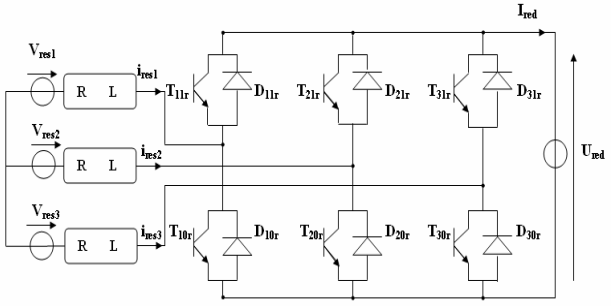

Fig.3: Structure of the two-level PWM current rectifier

A. Voltage feedback control

For each phase k (k=1, 2 or 3) of the three-phase network feeding, the rectifier considered can be represented by a R,L circuit. V_{resk} is the voltage of one phase k of the three-phase network and V_k is the voltage of the leg k of the rectifier [17].

The voltage loop imposes the effective value of the reference current of the network corresponding to the power exchanged between the network and the continue load (Fig 4).

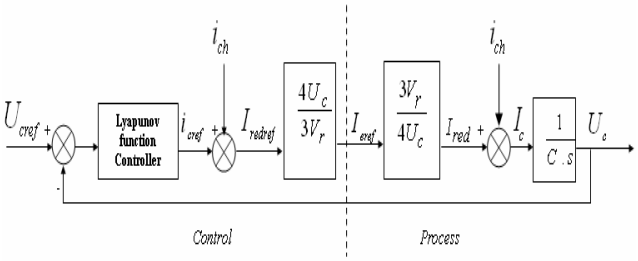

Fig.4: Control algorithm of the average output DC voltage of the two-level PWM current rectifier.

To guarantee the global asymptotic stability in the voltage loop, we obtain I_e as the output value of the voltage regulator:

$$I_e = \frac{4.U_C}{3.V_e}.\left[I_{ch} - K_U.C.(U_C - U_{Cref})\right] \qquad (6)$$

B. Current feedback control

We control the network current of the phase 1 and 2 by a sliding mode regulator. The algorithm of this current loop is given on the Fig 5. In this scheme, the transfer function $H(s)$ is expressed as follows:

$$H(s) = \frac{I_{resk}}{V} = \frac{1}{R + L.s} \qquad (7)$$

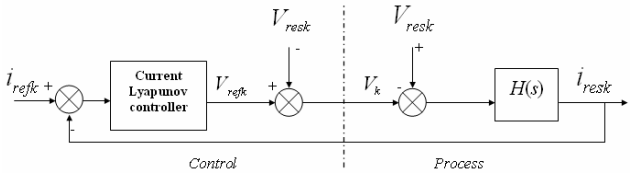

Fig.5: Control algorithm of the network current i_{resk} of the three-level PWM rectifier.

To guarantee the global asymptotic stability in the current loop, we obtain N_{gk} as the output of the current regulator:

$$N_{gk} = \frac{1}{4U_C}\left[V_{resk} - RI_{resk} - I_e\omega L\sqrt{2}\cos(\omega t - (k-1)\frac{2\pi}{3} + K_i L(i_{resk} - i_{refk})\right] \qquad (8)$$

IV. CLAMPING BRIDGE

In this section, a clamping bridge control is introduced to balance the four DC input voltages, avoid NP potential drift and improve the performances of the speed control of the permanent magnet synchronous machine.

Several publications have discussed ways to solve this balancing problem in three-level NPC-VSI [8-17]. The multitude of proposals (selection of appropriate voltage vectors) implemented to ensure DC voltage balancing can be broadly divided into two categories. In the first category based on space vector realization, redundant switching states of the converter are used while in the second category using carrier-based pulse width modulation (PWM) scheme, a zero sequence voltage signal is added to the modulation signals. In some schemes using zero sequence voltage to balance DC capacitor voltages, knowledge of load power factor (or direction of instantaneous power flow) is required which is difficult to implement under transient conditions, and in others, measurements of both capacitor voltages and load currents (magnitudes or polarities) are required. Unfortunately, these methods modify the output voltage waveform. Also, as the number of inverter-levels increases, the problem of capacitor balancing becomes more complex and the solution very drastic.

By using a separate supply for each DC-link level, the balancing issues are solved [6]. However, this solution is expensive especially for more then three-level. Another solution consists of adding electronic circuitry. In [16-18], clamping bridges based on transistors and resistors (dissipative method) are proposed as a solution to this problem. Advantages are low cost and low complexity. Disadvantages are high energy losses, high current switches and costly design thermal management requirements for large values. This method is best suited for systems that are charged often with small currents.

In order to remedy to the unbalance problem, we suggest a solution which consists in establish a bridge balancing between the rectifier and the intermediate filter (Fig 6). The aim of this use is to limit and stabilise variations of the input DC voltages of the inverter.

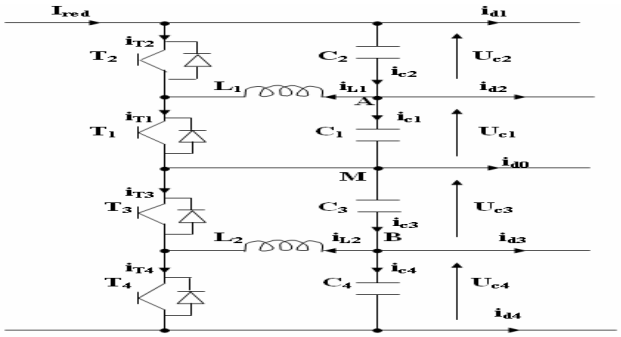

Fig. 6: Structure of the clamping bridge

The capacitor voltage equalization clamping bridge scheme has many advantages such as higher equalization efficiency and a modular design approach.

As shown in Figure 6, switches T_1 , T_2 , T_3 and T_4 are MOSFET; diodes D_1 , D_2 , D_3 and D_4 are continued flow diodes; L_1 and L_2 is the energy storage inductors; C_1 , C_2 , C_3 and C_4 are four adjacent series cells, respectively.

The basic operational principle is as follows:

* When $U_{c1}>U_{c2}$, a drive signal is given to the switches, and switch T_2 is turned off and T_1 is turned on. While T_1 is on, capacitor C_1, switch T_1 and inductor L_1 forms a loop circuit, whose current is I_{c1} . The part of energy of capacitor C_1 transfers to inductor L_1 . While T_1 is off, capacitor C_2 , inductor L_1 and the diode D_2 forms a loop circuit, whose current is I_{c2} .

  The energy of inductor L_1 transfers to capacitor C_2 .

* When $U_{c1} <U_{c2}$, switch T_1 is turned off and T_2 is turned on. The energy transfers from C_2 to C_1 until the voltages of the two capacitors are the same.

* When $U_{c3}>U_{c4}$, a drive signal is given to the switches, and switch T_4 is turned off and T_3 is turned on. While T_3 is on, capacitor C_3, switch T_3 and inductor L_2 forms a loop circuit, whose current is I_{c3}. The part of energy of capacitor C_3 transfers to inductor L_2 . While T_3 is off, capacitor C_4, inductor L_2 and the diode D_3 forms a loop circuit, whose current is I_{c2}. The energy of inductor L_2 transfers to capacitor C_3.
* When $U_{c3} <U_{c4}$, switch T_3 is turned off and T_4 is turned on. The energy transfers from C_3 to C_4 until the voltages of the two capacitors are same.

Capacitor voltage equalization control should be implemented to restrict the charge-discharge current to the allowable cell limitations in the capacitor string.

The balancing algorithm search to efficiently remove energy from a strong capacitor and transfer that energy into a weak one until the capacitor voltage is equalized across all capacitors.

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The balancing algorithms search to efficiently remove energy from a strong capacitor and transfer that energy into a weak one until the capacitor voltage is equalized across all capacitors.

A. Switch control strategy of the clamping bridge

Step 1: Deduction of the sign of the differences.

We use the following equations:

$$C_1 . \frac{d(U_{c1} - U_{c2})}{dt} = (i_{L1} - i_{c2} + i_{d2} + i_{c1}) \quad (9)$$

$$C_3 . \frac{d(U_{c3} - U_{c4})}{dt} = (i_{L2} - i_{c3} + i_{c4} + i_{d3}) \quad (10)$$

Step 2: Deduction of the command of the transistors

$$\begin{cases} U_{c2} > U_{c1} \Rightarrow T_2 = 1; T_1 = 0 \\ U_{c1} > U_{c2} \Rightarrow T_2 = 0; T_1 = 1 \\ U_{c3} > U_{c4} \Rightarrow T_3 = 1; T_4 = 0 \\ U_{c4} > U_{c3} \Rightarrow T_3 = 0; T_4 = 1 \end{cases} \quad (11)$$

V. Simulation Results

In order to validate the solution proposed previously, we present simulation results for the two-level PWM current rectifier – five-level NPC-VSI – PMSM cascade. In the first case, the clamping bridge will not be used in order to show the instability problem of the four input DC voltages. In the second one, the solution proposed is introduced to improve the performances of DC voltages and PMSM.

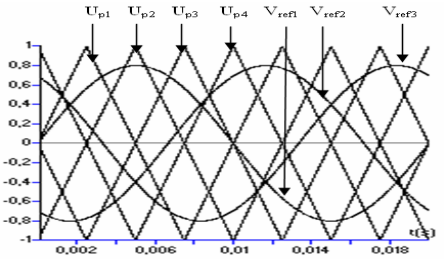

Fig.7. Reference voltages and bipolar carriers

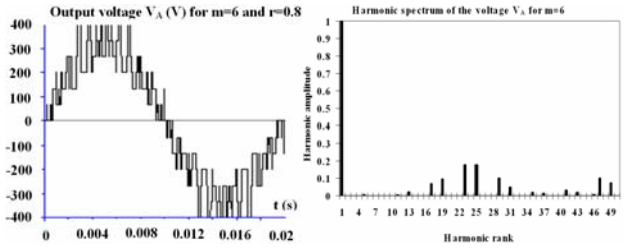

Fig.8. Output voltage V_A for m=6, r=0.8 and f=50Hz

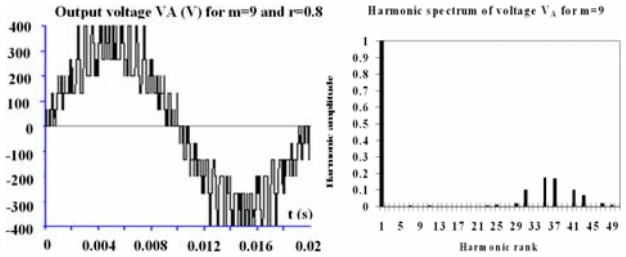

Fig.9. Harmonic spectrum of the voltage V_A (m=9 r=0.8.

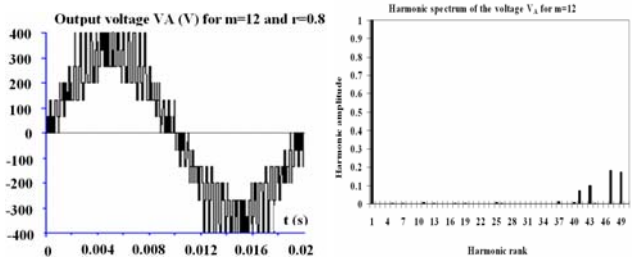

Fig.10. Harmonic spectrum of the voltage V_A for m=12 and r=0.8

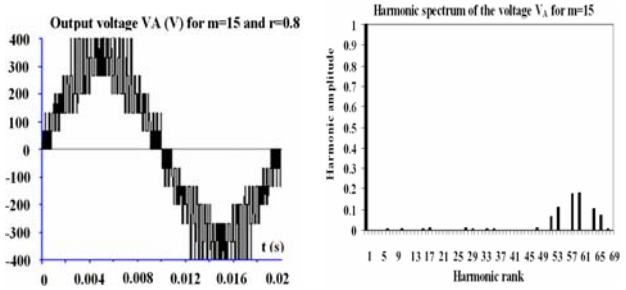

Fig.11. Harmonic spectrum of the voltage V_A for m=15 and r=0.8

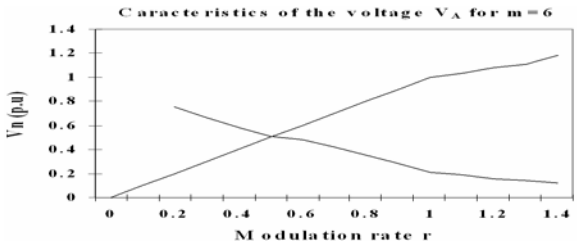

Fig.12. Characteristics of the voltage V_A for m=6

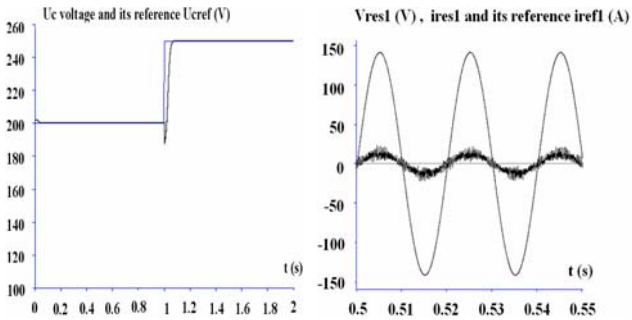

Fig.13: Voltage U_c and its reference and the network voltage V_{res1} , the network current i_{res1} and its reference i_{ref1}

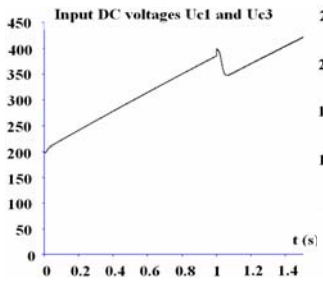

Fig.14: Voltage U_{c1} and Uc3

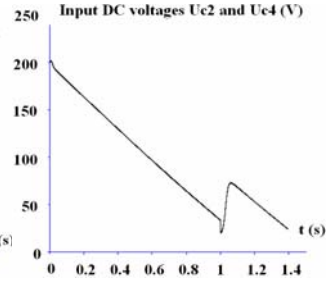

Fig.15: Voltage U_{c2} and Uc4

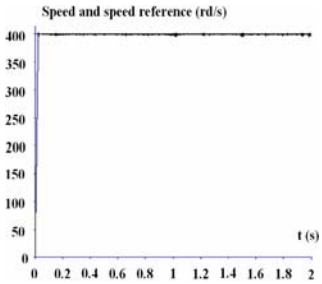

Fig.16: Speed and its reference

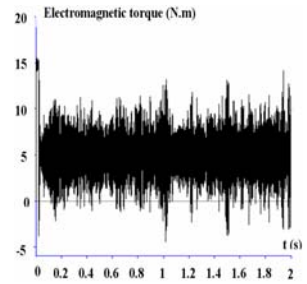

Fig.17: Electromagnetic torque

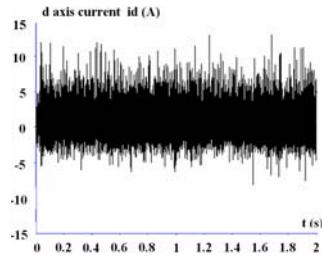

Fig.18: d axis current (i_d)

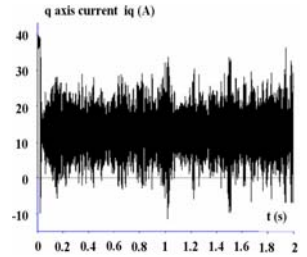

Fig.19: q axis current (i_q)

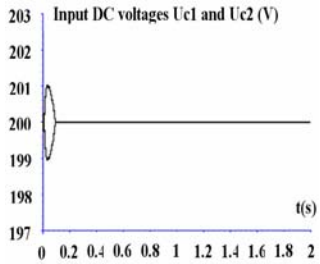

Fig.20: Voltages U_{c1} and U_{c2}

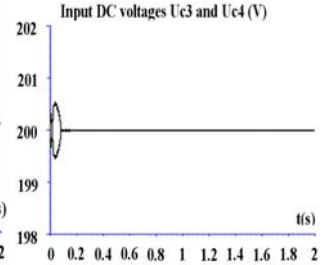

Fig.21: Voltages U_{c3} and U_{c4}

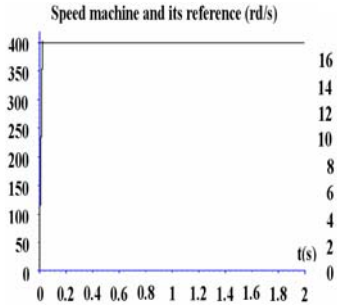

Fig.22: Speed and its reference

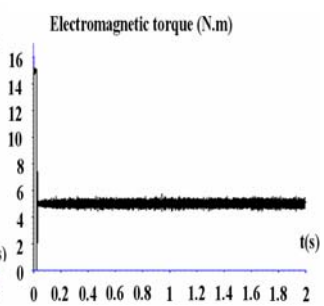

Fig.23: Electromagnetic torque

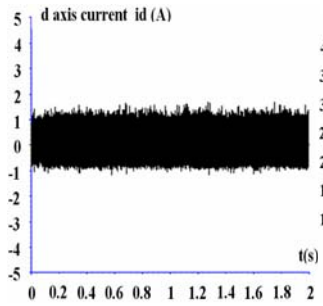

Fig.24: d axis current (i_d)

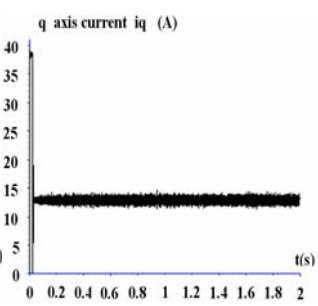

Fig.25: q axis current (i_q)

VI. Results and Discussions

The figure 7 shows the reference voltages and the four bipolar carriers used for this strategy. The figures 8 to 11 give the output voltage V_A. and its harmonic spectrum for a modulation index m=6 (Fig.8), m=9 (Fig.9), m=12 (Fig.10) and m=15 (Fig.11) and a modulation rate r=0.8. The frequency is 50 Hz. We notice that in the four cases, the harmonics gather by families centred around frequencies multiple of 4.m.f. Because of the symmetry to the quarter of the period presented by the voltage V_A, we obtain only odd harmonics. The most important harmonics gather around the first family.

The modulation rate r lets linear adjusting of fundamental magnitude from r=0 to r=1 and the harmonics rate decreases when r increases (Fig.12).

For evaluating the performances of the Clamping bridge proposed, two simulations are presented. The first one propose to study a one two-level PWM current rectifier – Five-level NPC VSI – Permanent Magnet Synchronous Machine. This study shows particularly the problem of the instability of the input DC voltages of the five-level NPC VSI and its consequence on the performances of the PMSM speed control for U_{DC}=800V, m=72, r=0.8

In order to test the Lyapunov function control of the average value of the output voltage of the two-level PWM rectifier, a voltage reference of 200V is applied and at t=1s we increase this reference from 200 to 250V. The figure 13 shows the voltage U_c and its reference obtained. This voltage follows perfectly its reference (200V). The network current i_{res1} of the rectifier is in phase with the network voltage V_{res1}. The parameters of the net are: R=0.25Ω ; L=10mH.

On the figure 14 and 15, we show perfectly the problem of the unbalance of the four DC voltages of the intermediate capacitors bridge. The voltages U_{c2} and U_{c4} are decreasing and the voltages U_{c1} and U_{c3} are increasing. The parameters of the capacitors are: C_1=C_2=C3=C4= 20µF

The figures 16 to 19 show the consequences of the DC voltages drift on the characteristics of the Permanent Magnet Synchronous Machine. The speed follows its reference (400 rd/s) but the undulations on the electromagnetic torque and different currents (i_d, i_q) are very important due to the unbalance problem of the four input DC voltages. The parameters of the PM synchronous machine are: L_d=L_q=3.2mH; R_s=1Ω; p=3; Φ_f=0.13N.m/A; J=6.10^{-4} kg.m²; F_c=$9{,}5.10^{-5}$ N.m.s/rad.

Those results show the importance of the stability of the input DC voltages of the inverter in order to have good performances for the speed control of the PM synchronous machine.

On the second simulation, we introduce the clamping bridge proposed in the precedent cascade on the Figure 1 in order to show the different input DC capacitor voltage equalization performances. We can see on the figures 20 and 21 that the four voltages (U_{c1}, U_{c2}, U_{c3} and U_{c4}) stabilise around the reference voltage value (200V) and the DC link capacitor voltages are equalized. By using this technique of stabilisation, we can remark on the figure 22, 23, 24 and 25 that the undulations on the performances (Torque and currents i_d and i_q) of the PMSM disappear and those performances are improved by using the inductive Clamping bridge. The parameters of the Clamping bridge are: L_1= 1mH L_2=1mH.

The afore-presented results confirm that the clamping bridge is able to equalize DC link capacitor voltages and stabilize the different DC voltages around the desired value. The performances of speed control of the PMSM are then ameliorating.

VII. CONCLUSION

The present contribution intends to demonstrate that permanent magnet synchronous machine control based on sliding mode control when applied with a two-level PWM current rectifier – Five-level PWM NPC-VSI may contribute both for functional performances improvement and attenuation of some technological limitations. The input DC voltages are generated by a two-level PWM current rectifier controlled by Lyapunov function. By this study, we have particularly shown the problem of the stability and its effects on the speed control of PMSM and the input DC voltages sources of the inverter.

In the last part of this paper, we propose a simple solution to stabilise the four DC voltages and this by using a clamping bridge composed by four switches (pair transistor-diode) and two inductances.

This nondissipative equalization design has many advantages such as high equalization efficiency due to the nondissipative current diverter, bidirectional energy transferring capability, and a modular design. Another advantage of this system is that no closed-loop control is needed and the process is self-limiting: when voltage equalization is complete, the switching of the capacitors consumes minimal energy.

APPENDIX

L_d , L_q : self inductance of the d and q armatures equivalent winding, R_s : resistance of an armature winding, ω : angular speed. s : Laplace operator,

J : inertia of the set machine-load , C_r : Load torque,

e_d : Error variable, S_d : Surface variable

V_{resk} : Network voltage of one phase k, V_k : Voltage of the leg k of the rectifier, R : grid resistance L : grid inductance

U_C : Average value of the four input DC voltages

C_1, C_2, C_3, C_4 : input capacitors of the five-level NPC-VSI

$V_{res}; i_{res}$: Voltage and current of the grid

V_e : Effective value of the grid voltage

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Implementation of Three phase Shunt Hybrid Filter Using ICOSϕAlgorithm

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Abstract– This paper presents a hybrid filter configuration to suppress harmonic current distortion in the source current. It is a combination of shunt active power filter and shunt passive filter. Major amount of harmonic currents generated by the nonlinear load are bypassed through the passive filter and the active power filter supplies the remaining harmonics and reactive power. Thus the power rating of the shunt active power filter can be reduced in the hybrid configuration compared with pure active filter configuration. The effectiveness of the adopted topology and control scheme has been verified by simulation and experimental results under various source/load conditions.

Keywords– Hybrid filter, Power quality, Harmonic compensation.

I. INTRODUCTION

A large number of solid state power converters such as diode bridge rectifiers and thyristor converters are used in industrial applications and transmission/distribution networks. All these breeds of power converters are nonlinear in nature and cause serious problems of current harmonics, poor power factor, non sinusoidal supply voltage, reactive power burden and low system efficiency. Hence, due to these serious issues there has been an increasing interest in the subject of power quality improvement techniques which can suppress supply harmonics, improve power factor and balance the input supply [1].

Many circuit configurations of filters have been suggested to limit harmonic current distortion. Passive filters which act as least impedance path to the tuned harmonic frequencies were used initially to reduce harmonics. This technique is simple and less expensive. But it has many drawbacks such as resonance, fixed compensation characteristics, bulky size, high no load losses etc. As a better option of complete compensation of distortions, active power filters [2, 3] have been researched and developed. Active filters overcome drawbacks of passive filter by using the switched mode power converter to perform complete harmonic current elimination. Shunt active power filters are developed to suppress the harmonic currents and reactive power compensation simultaneously by suitable control techniques to generate a compensating current in equal and opposite direction so that source current becomes harmonic free[2,4].

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However, the power rating and construction cost of active power filters in a practical industry is too high. To avoid this limitation, hybrid filter topologies have been developed. Using low cost passive filters with the active filter, the power rating of active converter is reduced compared with that of pure active filters. This hybrid filter retains the advantages of active filters and passive filters. Also hybrid filters are cost effective and become more practical in industry applications [5-9].

In this paper, the hybrid filter structure consisted of an active filter and a passive filter, connected in shunt is used for power quality improvement. The effectiveness of the hybrid filter configuration was verified with simulation and experimental results. The results prove that the proposed method can effectively eliminate harmonic currents, balance source currents, compensate reactive power i.e. in other words; power quality improvement of the power system is achieved by the proposed hybrid filter structure and control method.

II. STRUCTURE OF HYBRID FILTER CONFIGURATION

The hybrid filter structure consists of shunt passive filter and shunt active filter. Shunt passive filter is a series combination of a capacitor and a reactor tuned to a specific harmonic frequency. It provides low impedance trap to harmonic to which the filter is tuned, usually to lower order harmonics because the major contribution of harmonics is due to lower order harmonics. Remaining higher order harmonics only are to be filtered by shunt active filter; hence its power rating can be reduced. A three phase voltage source inverter (VSI) is used as the shunt active filter. The hybrid filter is connected in parallel with the nonlinear load. The diagram of hybrid filter structure is shown in the fig.1.

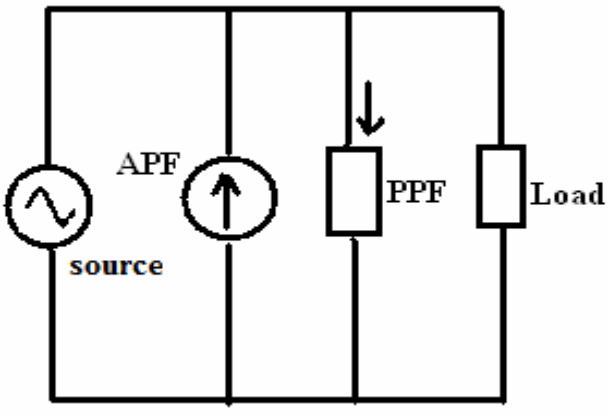

Fig.1. The shunt hybrid filter structure

The nonlinear loads considered in this study are three phase diode bridge rectifier and three phase thyristor converter. A proportional integral voltage controller is used to maintain the constant dc link voltage of the inverter. A hysterisis current comparator is used to track the output current to generate proper PWM pulses to the inverter.

III. Control Strategy of Shunt Active Filter

Various control algorithms were developed in literature such as instantaneous reactive power theory, synchronous detection, dc bus voltage algorithm etc [2]. The instantaneous reactive power theory and synchronous detection algorithm operates satisfactorily under balanced conditions only. In this work, ICOSΦ algorithm is used which is tested satisfactorily under distorted and transient conditions[4,10,11].The shunt active filter uses *ICOSϕ* algorithm, In *ICOSϕ* algorithm, mains required to supply only the real component of the load current, remaining parts of load current – reactive component and harmonics – is to be supplied by the active filter [4]. The extraction of real component of load current can be done as follows:

The load current contains fundamental component and harmonic components. The lower order tuned frequency components are filtered by the passive filters. Remaining harmonic components are filtered with active filter. These harmonics are sensed with the help of low pass (biquad) filter. Its output is fundamental component delayed by 90° (i.e. i_m sin (ωt -ϕ -90°)). At the time of negative zero crossing of the input voltage, i.e.,ωt = 180°, instantaneous value of fundamental component of load current is i_m cosϕ.The magnitude of the desired source current $|I_{s(ref)}|$ can be expressed as the magnitude of real component of the fundamental load current in the respective phases. i.e. for phase a it can be written as $|I_{s(ref)}| = |\mathrm{Re}(I_{La})|$.

The desired (reference) source currents in the three phases are given as,

$$i_{sa(ref)} = |I_{s(ref)}| \times U_a = |I_{s(ref)}|.\sin \omega t$$

$$i_{sb(ref)} = |I_{s(ref)}| \times U_b = |I_{s(ref)}|.\sin(\omega t - 120^0)$$

$$i_{sc(ref)} = |I_{s(ref)}| \times U_c = |I_{s(ref)}|.\sin(\omega t + 120^0) \qquad (1)$$

The compensation currents to be injected by the shunt active filter are the difference between the actual load currents and the desired source currents.

$$i_{a(comp)} = i_{La} - i_{sa(ref)}\,; \quad i_{b(comp)} = i_{Lb} - i_{sb(ref)}\,;$$

$$i_{c(comp)} = i_{Lc} - i_{sc(ref)}\,; \qquad (2)$$

IV. Simulation Results

As case studies, three phase diode bridge rectifier and three phase thyristor converter are considered as harmonic loads.

Case I: Diode bridge Rectifier Load

A three-phase 400 V, 50 Hz balanced supply is given to a 15kW AC-DC Diode bridge rectifier feeding a variable inductive load. The MATLAB model of the system is shown in Fig.2.

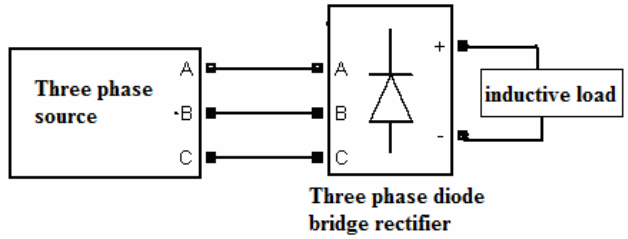

Fig.2: The three-phase system with diode bridge rectifier

A. Without filter:

The performance of diode bridge rectifier feeding an inductive load was studied without any filter in the system. The system was simulated under balanced source and balanced load conditions. The source current is highly distorted.

B. With passive filter:

The 5th and 7th order of shunt passive filters are designed to sink in respective harmonic currents. The capacitors for the passive filter are selected to supply the specified percentage of the reactive power requirement of the load. The MATLAB model of the system with passive filters is shown in Fig.3.

Table 1: Parameter values of passive filter

Harmonic	Resistor	Inductor	Capacitor
5th	0.0314Ω	10mH	40μF
7th	0.0160Ω	5.1mH	40μF

Table 1 gives the parameter values of passive filter components for compensation.

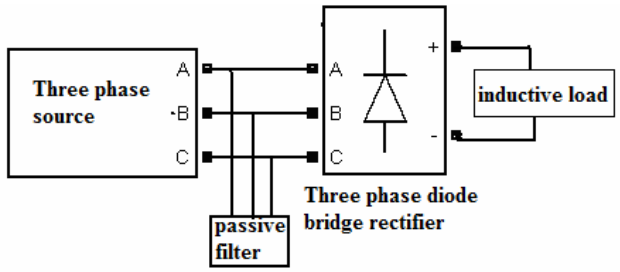

Fig.3: Simulation model of the three-phase system with Passive filter

The passive filter helps to reduce the major amount of distortions in source current. i.e., the passive filter sinks the 5th and 7th harmonic currents by providing a low impedance path.

C. With Active Filter

In the next stage, the simulation is repeated with the shunt active filter in the system. The circuit for ICOSφ [4]

algorithm was simulated in MATLAB/SIMULINK and installed in the system. The MATLAB model of the system with active filters is shown in Fig.4.

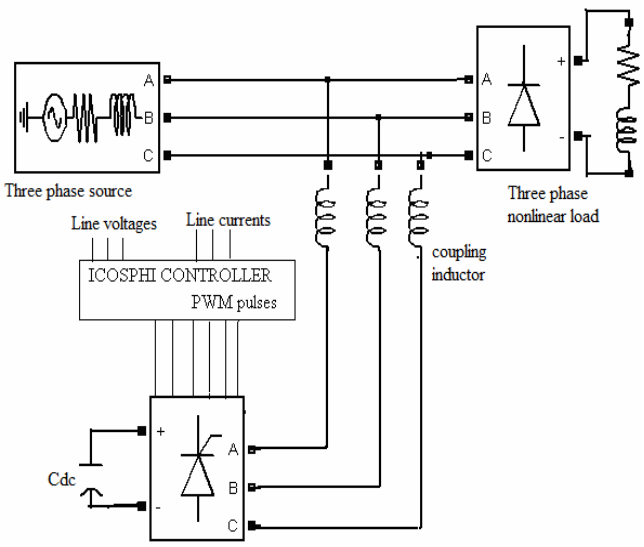

Fig.4: Simulation model of the three-phase system with I COSϕ controller based shunt active filter

Simulation results with addition of active filter are shown in Fig.5.The harmonics in source current is highly reduced and THD is within standard limits. The source voltage and source current are in phase and sinusoidal, and implies perfect reactive compensation. Certainly, it takes time delay more than 1 cycle for perfect compensation.

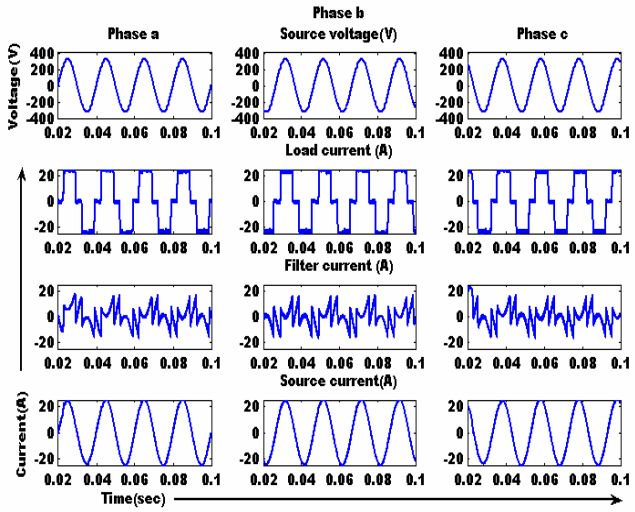

Fig.5: Source voltage and source current of three-phase system with shunt active power filter – for the diode bridge rectifier load.

C. With Hybrid Filter

Hybrid system uses a shunt passive filter to remove the lower order harmonics and a shunt active filter to remove the remaining harmonics and reactive power compensation. The shunt active filer uses the ICOSφ control algorithm. The fig.6 is the simulation model of the three phase system with hybrid filter.

The total harmonic distortion with hybrid filter is reduced to 0.47% and source current becomes in phase with source voltage. Fig.7 shows waveforms of source voltage, load current, source current waveforms of diode bridge rectifier load with hybrid filter.

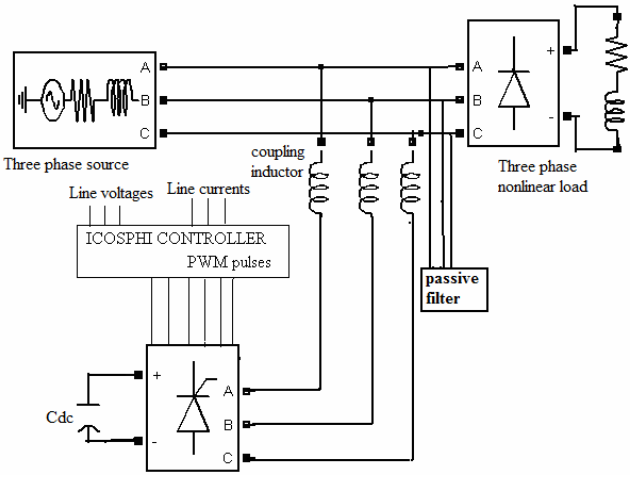

Fig.6: Simulation model of the three-phase system with Hybrid filter.

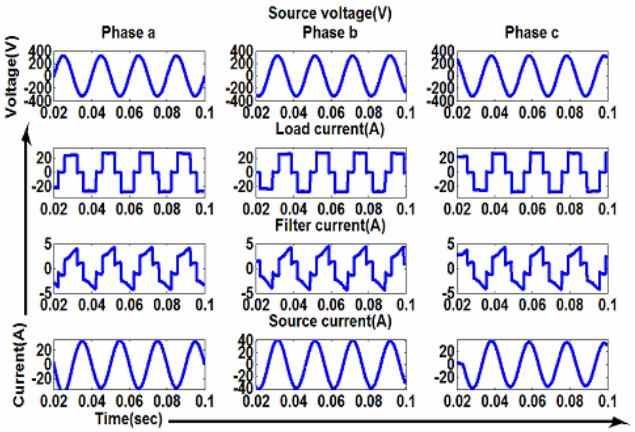

Fig.7: Source voltage, load current and source current of three-phase system with hybrid filter- for diode bridge rectifier load

The simulation results for diode bridge rectifier load are summarized in Table 2. The comparative study shows that hybrid filter much effectively reduces harmonic distortion in the source current with effective reactive power compensation. The performance of the shunt hybrid filter was verified experimentally with diode bridge rectifier.

Table 2: Performance of various filter configurations with diode bridge rectifier

Parameters	Without filter	With Passive filter	With Active filter	With Hybrid filter
Fundamental source current in rms (A)	16.87	21.47	17.04	18.55
THD in Source Current (%)	18.45	1.62	0.91	0.47

V. ANALOG CIRCUIT IMPLEMENTATION OF HYBRID FILTER

A laboratory model of the shunt hybrid filter - ICOSϕ controller based shunt active filter and shunt passive filter - was set up for testing with the nonlinear load, three phase diode bridge rectifier. Fig.8 shows the hardware set up for the experiment. A voltage source inverter assembly, which consists of a three phase IGBT based inverter along with large DC link capacitor, is used as the shunt active filter. DC link capacitor of 1650mF / 800V is used to maintain steady voltage required by the inverter.

Fig.8. Hardware setup

The operations in the analog circuit can be explained as follows:

Step 1: The source voltages, load currents and active filter injection currents are sensed with hall effect voltage and current sensors.

Step 2: Detection of fundamental component of load current:

Low pass filtering by using biquad filter is done to extract fundamental component of load current. The advantages of using biquad filter, rather than other low pass filters, are it is easy to design, gives unity gain and exact 90° phase shift.

Step 3: Determination of real component of load current:

The circuit with the comparator and monostable multivibrator 74LS123 is used for getting sharp output pulses at the negative zero crossing of the phase voltage. These pulses and output of the biquad filter are fed to a sample and hold circuit to obtain instantaneous value of fundamental component of load current at negative zero crossing of source voltage, i.e., real part of load current .

Step 4: Obtaining desired source current waveforms:

The real component of load current is multiplied with unit sinusoidal waves to obtain desired source current waveforms, using AD 633 JN multiplier.

Step 5: Derive PWM pulses to inverter:

The reference compensation current is obtained by subtracting reference source current from load current. A comparator is used to compare reference compensation current and actual filter current. When reference filter current is more than actual filter current, output of the comparator is high and vice versa. The comparator is realized using op-amp 741 and IC 4049B. The isolation between power circuit and controller circuit is done using an optocoupler 6N136. The output pulses are amplified using transistor amplifier BC 547[4].

Based on reactive power requirement of the system under the rated load condition, passive LC filters are designed and inserted. The components of passive filters – inductor and capacitor – are designed for 6^{th} harmonic frequency, such that major amount of 5^{th} and 7^{th} harmonics can be eliminated with a single tuned passive filter.

VI. EXPERIMENTAL STUDY

The experimental results on a scaled down balanced three phase system connected to diode bridge rectifier feeding a resistive load (230V, 3kW) are presented in this section.

The passive filter is designed for 100% Var compensation and it is tuned to the sixth harmonic so as to avoid resonance condition and to sink both 5^{th} and 7^{th} harmonic currents to certain extent. This will reduce the size of the passive filter and hence the loading on the source also. In this case study, combination of passive filter elements used is 5mH-80μF.

The ICOSφ controller senses load current, supply voltage and generate PWM pulses to IGBT inverter. The shunt active power filter is connected to three phase supply at point of common coupling through 10mH, coupling reactance. The system was operated under various source/load conditions and the results are shown in the following section. The test results are analyzed using FLUKE make *power quality analyzer*.

A: Balanced Source Balanced Load

The hybrid power filter, combination of shunt active and shunt passive filters, reduces total harmonic distortion in source current.

Passive filter reduces the lower order (5^{th} and 7^{th}) harmonics and the shunt active power filter injects the remaining harmonics in source current.Relevant results are shown in Fig.9 and Fig.10.

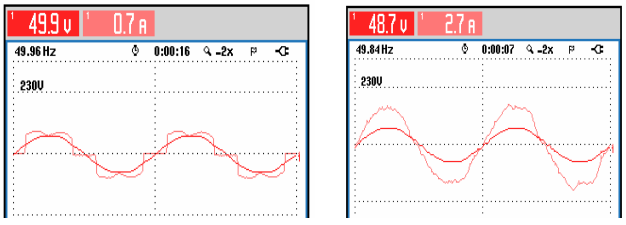

Fig.9: a-phase source voltage and source current
a) without hybrid filtering b) with hybrid filtering

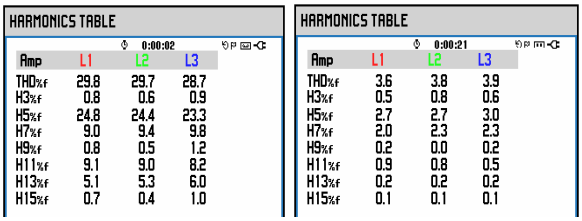

Fig 10: a) Harmonic spectrum of source current
a) without hybrid filtering b) with hybrid filtering

B:Distorted source and Balanced Load

The distorted source voltages are applied across the diode bridge rectifier feeding resistive load. When there is distortion in the supply voltages, the fundamental components are first derived using suitably tuned second order low pass filters to make the voltages balanced and sinusoidal. The unit sine wave of these balanced voltages are used as templates as required by the ICOSφ algorithm to generate compensation currents. The experimental results are shown in Fig 11 and Fig 12.

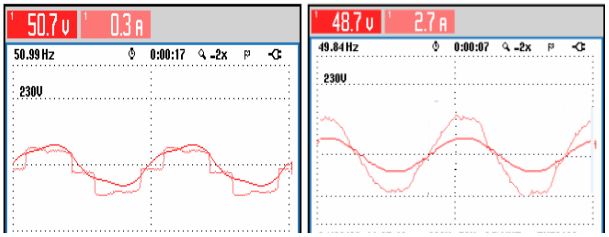

Fig.11: a-phase source voltage and source current
a) without hybrid filtering b) with hybrid filtering

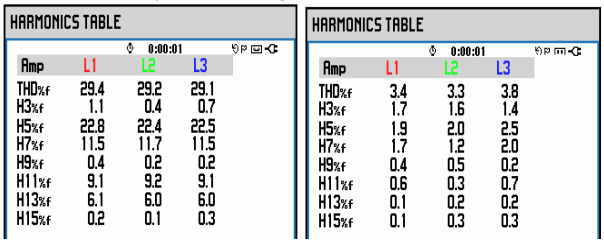

Fig 12: Harmonic spectrum of source current
(a) without hybrid filtering (b) with hybrid filter

C. Balanced source Unbalanced Load

The unbalance in three phase currents are introduced by a star connected unbalanced resistive load in shunt with diode bridge rectifier. The shunt active filter using the ICOSφ algorithm makes sure that the source currents in all the same phases remain balanced even in case of load unbalance. The active filter along with the passive filter reduces the THD in source currents and the experimental results are shown in Fig 13 and Fig 14.

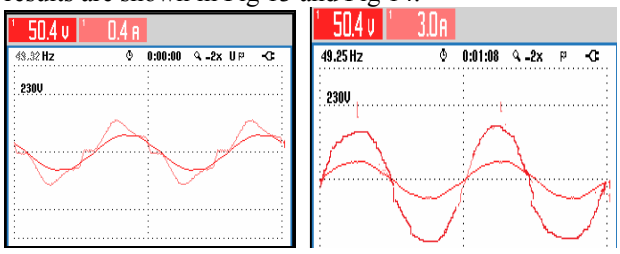

Fig.13: a-phase source voltage and source current
(a) without filtering b) with hybrid filtering

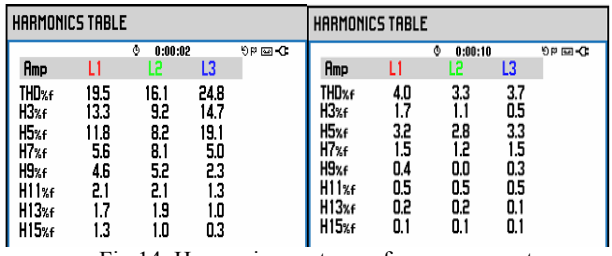

Fig 14: Harmonic spectrum of source current
(a) without hybrid filtering (b) with hybrid filtering

The experimental results are summarized in Table 3.
Table 3 compares the performance of the test system with and without hybrid filtering. It can be seen that harmonics in the source current is highly reduced with the addition of the hybrid filter. Also it is calculated that size of the active filter can be reduced up to 30% in this hybrid configuration.

Table 3: Performance of various filter configurations with diode bridge rectifier

	THD in source current (%)					
	Without hybrid filter			With hybrid filter		
	R	Y	B	R	Y	B
Balanced Source And Load	29.8	29.7	28.7	3.6	3.8	3.9
Distorted Source And Balanced Load	29.4	29.2	29.1	3.4	3.3	3.8
Balanced Source Unbalanced Load	19.5	16.1	24.8	4.0	3.3	3.7

VII. Conclusion

With the development of more sophisticated power electronic nonlinear devices, more and more power quality issues were initiated. As remedies to these problems, many filtering techniques such as passive filter, active filter, hybrid filter etc. are developed. The simulation results show the shunt hybrid filter is much superior in performance compared to other configurations. The three-phase hybrid filter is implemented in hardware as combination of shunt passive filter and shunt active filter. The three-phase hybrid filtering system works quite efficiently under various source/load conditions such as balanced supply and balanced load, distorted source and balanced load ,balanced supply and unbalanced load etc.

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PI with Fuzzy Logic Controller based Active Power Line Conditioners

Karuppanan P.[1] Kamala Kanta Mahapatra[2]

Abstract –This paper presents a proportional integrator (PI) in conjunction with Fuzzy Logic controller (FLC) based Shunt active power line conditioners (APLC) for power quality improvements. The objective is to investigate different control methodologies for real time compensation of current harmonics and reactive power due to non-linear loads at various power conditions. The compensation process includes controlling dc-bus capacitor voltage of the inverter and estimating peak reference current by using PI with fuzzy logic controller. The reference currents are extracted from unit sine vector multiplied with estimated peak reference current. The voltage source inverter switching signals are obtained through hysteresis current controller (HCC). The performance of shunt APLC is evaluated through Matlab/Simulink simulation under different steady state and transient conditions using PI, FLC and PI in conjunction with FLC. The results demonstrate that combination of PI with FLC is a better solution that reduces the settling time of the dc-bus capacitor and suppresses current harmonics in the loads.

Keywords – Shunt Active Power Line Conditioners (APLC), PI controller, Fuzzy Logic Controller (FLC), Harmonics, Hysteresis Current Controller (HCC).

I. INTRODUCTION

The ac power supply feeds different kind of linear and non-linear loads. The non-linear loads produce harmonics and reactive power related problems [1]. This harmonics and reactive power cause poor power factor and distort the supply voltage at the point of common coupling (PCC). This distortion is mainly induced due to the line impedance or distribution transformer leakage inductance. The current harmonics create problems in power systems such as malfunctions in sensitive equipment, overvoltage by resonance and harmonic voltage drop across the network impedance; that result in poor power factor [2]. Traditionally these problems are solved by passive filters. But these passive filters introduce tuning problems, resonance, and are large in size and it's also limited to few harmonics [3-4]. Recently active power-line conditioners (APLC) are developed to compensate the current harmonics and reactive power simultaneously in addition to power factor correction [5]. APLC keeps the mains current balanced after compensation regardless of either the load is non-linear and/or unbalanced [6]. The shunt APLC can be developed with current source inverter or voltage source inverter. Generally the voltage source inverter (VSI) is preferred for the shunt active power circuit due to lower losses in the dc-side capacitor [7].

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The controller is the most important part of the APLC and currently lot of research is being conducted in this area [8-10]. Conventional PI and proportional integral derivative (PID) controllers have been used to estimate the peak reference currents and control the dc side capacitor voltage of the inverter. Most of the active filter systems use PI-controller for maintaining the dc side capacitor voltage [5-11]. When the source supplies a non-linear or reactive load, it is expected to supply only the active fundamental component of the load current and the compensator supplies the harmonic/reactive component. The outer capacitor voltage loop will try to maintain the capacitor voltage nearly constant which is also a mandatory condition for the successful operation of the APLC. The system losses are provided by the source in steady state. The compensator supplies the harmonic power, which manifests itself only on the reactive component of power. In the transient conditions the load changes are reflected in the dc capacitor voltage as an increase (or decrease) as capacitor absorbs (or delivers) the excess (or deficit) power. This conservation of energy philosophy is used to obtain the reference current for compensator in this method. The perturbations in the capacitor voltage are related to the perturbations in the average power drawn by the non-linear load. This property is utilized which facilitates extracting compensator reference and maintains capacitor voltage. However, the conventional PI controller requires precise linear mathematical model of the system, which is difficult to obtain under parameter variations and non-linear load disturbances. Another drawback of the system is that the proportional and integral gains are chosen heuristically [12-13]. Recently, fuzzy logic controllers (FLC) are used in power electronic systems and active power filter applications [14-18]. In the present work we combine PI and FLC techniques for efficient power line conditioning. This controller can handle non-linearity and is more robust.

This research paper presents a novel controller that uses PI in conjunction with Fuzzy logic controller for active power line conditioner. The proposed PI with fuzzy logic controller is used to estimate peak reference current besides maintaining the DC side capacitor voltage of the inverter nearly constant. Hysteresis current controller is used to generate the switching signals for switches in the inverter. The shunt APLC is investigated under different steady state and transient conditions using PI, FLC and PI in conjunction with FLC and is found to be effective for compensation; the proposed PI with FLC reduces ripples in the dc side capacitor.

II. DESIGN OF SHUNT APLC

The basic compensation principle of shunt APLC is to draw/supply compensating current**,** from/to the distributor system such that it cancels current harmonics on the

source side and makes the source current sinusoidal and is in phase with the source voltage. The active power filter is implemented with pulse width modulated (PWM) current controlled voltage source inverter (VSI). The three phase APLC consists of six power transistors with freewheeling diodes, a dc capacitor, RL filter, compensation controller (PI or FLC or PI in conjunction with FLC) and gate signal generator (hysteresis current controller) as shown in the Fig 1. These PI and Fuzzy logic controller algorithm is used to extract the desired reference current from the load current. The hysteresis current controller is employed to generate the switching signals for driving switches in the VSI. The inductive-filter suppresses the harmonics caused by the switching operation of the IGBT inverter. This inductive-filter provides smoothing and isolation for high frequency components. The current wave shape is limited by the switching frequency of the voltage source inverter.

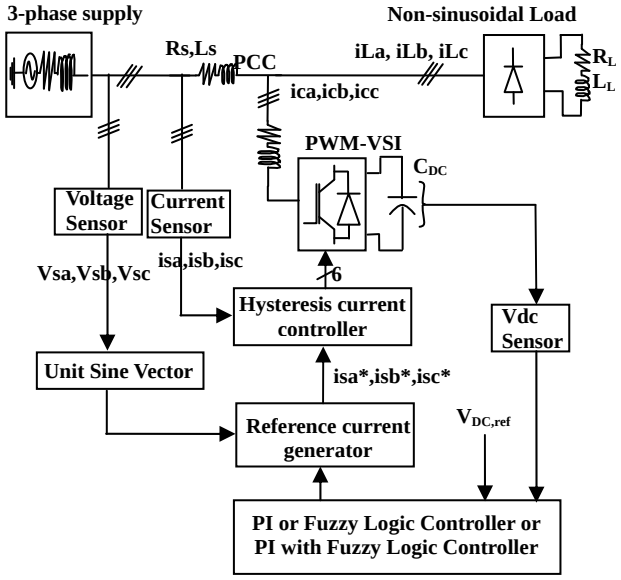


Fig. 1 structure of Shunt APLC system

The three phase source is connected to a diode rectifier (non-linear) load. This nonlinear load current contains fundamental component and higher order of harmonic current components. For this system, the instantaneous load current can be written as follows

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Phi_n)$$

$$= I_1 \sin(\omega t + \Phi_1) + \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) \quad (1)$$

The load power comprises fundamental power and reactive power including harmonic power. The instantaneous load power can be written as

$$p_L(t) = i_s(t) * v_s(t)$$

$$= V_m \sin^2 \omega t * \cos\phi_1 + V_m I_1 \sin \omega t * \cos \omega t * \sin \phi_1$$

$$+ V_m \sin \omega t * \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right)$$

$$= p_f(t) + p_r(t) + p_h(t) \quad (2)$$

Here $p_f(t)$ is the fundamental component of power, $p_r(t)$ is the reactive power and $p_h(t)$ represents harmonic power. From this equation only the real (fundamental) power drawn by the load is

$$p_f(t) = V_m I_1 \sin^2 \omega t * \cos\phi_1 = v_s(t) * i_s(t) \quad (3)$$

The source current drawn from the mains after compensation should be sinusoidal; this is represented as

$$i_s(t) = p_f(t) / v_s(t) = I_1 \cos\phi_1 \sin \omega t = I_{\max} \sin \omega t \quad (4)$$

If the active power line conditioner provides the total reactive and harmonic power, source current $i_s(t)$ will be in phase with the utility voltage and would be sinusoidal. At this time, the active filter must provide the compensation current:

$$i_c(t) = i_L(t) - i_s(t) \quad (5)$$

APLC estimates the fundamental from the load current and compensates for the harmonic and reactive component.

Design of DC side capacitor:
The DC-side capacitor voltage is maintained constant with small ripples in steady state. It acts as energy storage element to supply real power (difference between load and source) during the transient period as already presented in the introduction. The real/reactive power injection results in the ripple voltage of DC capacitor. The selection of C_{DC} should be such that it facilitates reducing voltage ripple.

Design of filter inductance L_C and reference voltage:
The design of the filter inductance (L_C) and reference voltage ($V_{DC,ref}$) components is based on the following assumption; (1) The ac source voltage is sinusoidal (2) To design L_C the ac-side line current distortion is assumed to be *5%.* (3) Fixed capability of reactive power compensation of the APLC. (4) The PWM-inverter is assumed to operate in the linear modulation index (*i.e.*$0 \le m_a \le 1$) . The desired reference voltage is compared with actual dc-bus capacitor voltage for reducing the ripples in transient conditions.

III. Proposed Control Strategies

The proposed control strategy consists of extracting reference current and hysteresis current controller for IGBT inverter. The reference current is extracted from the nonlinear load current. The magnitude of the reference current is estimated by PI or FLC or PI with fuzzy logic controller.

A) Reference current control strategy:

The reference current generation is based on estimated peak reference currents that are multiplied with unit sine vector outputs. The proposed PI with fuzzy logic controller is used to estimate the peak reference current.
A.1) Unit sine vector:
The voltage source is converted to the unit current(s) while

corresponding phase angles are maintained. According the ohms law the current is inversely proportional to the resistance $(i = V / R)$. Unit sine vector is derived from the supply voltage template.

$$i_a = \sin \omega t, i_b = \sin(\omega t - 120^0),\ i_c = \sin(\omega t + 120^0) \qquad (6)$$

The amplitude of the sine current is unit or 1 volt and frequency same source voltage and it is also in the same phase. This unit current multiplied with peak value of control output generates reference current.

A.2) PI with Fuzzy controller:

Figure 2 shows the block diagram of the proposed proportional integral (PI) control with fuzzy logic controller scheme for APLC. The DC-side capacitor voltage is sensed and is compared with a reference voltage signal and generates error signal. The error signal $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as input to the PI-controller.

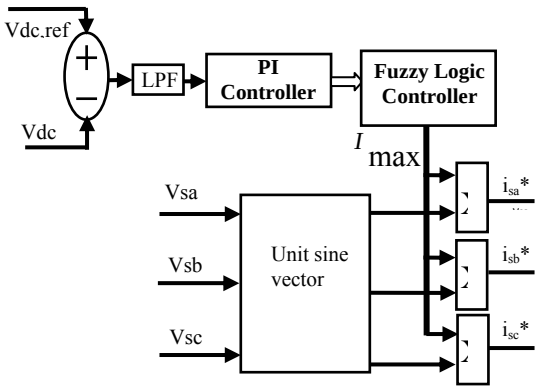


Fig. 2 PI with fuzzy logic Controller block diagram

The error signal passes through Butterworth low pass filter (LPF) that suppresses higher frequency components and allows only fundamental components. PI-controller estimates the magnitude of peak reference current $I_{\max}$ and controls the dc-side capacitor voltage of the inverter. Its transfer function is

$$H(s) = K_P(s) + \frac{K_I}{s} \qquad (7)$$

where, [K_P =0.7] is the proportional constant that determines the dynamic response of the DC-side voltage and [K_I =23] is the integration constant that determines it's settling time. The PI controller output contains certain ripples, so we need another processing unit to reduce this ripple; the FLC is connected together with PI controller for reducing the ripples.

Fuzzy logic controller block diagram shown in Fig 3, the transition between membership and non membership functions can be gradual. The PI controller output error is used as inputs for FLC. The linguistic variables are error $E(n)$, change of error $CE(n)$ and output $I_{\max}$.

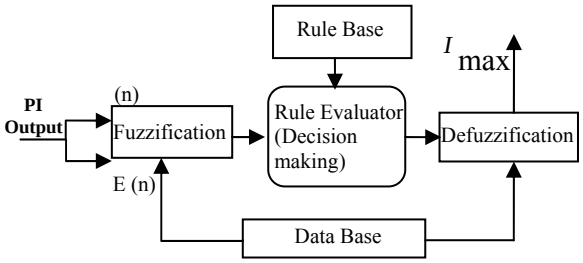
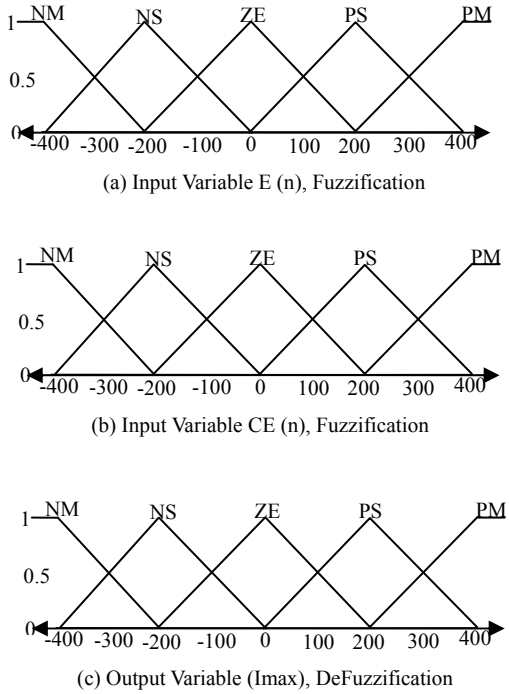


Fig. 3 fuzzy logic Control block diagram

Fuzzification:

In a control system, error between reference and output can be labeled as zero (ZE), positive small (PS), negative small (NS), positive medium (PM), negative medium (NM). The process involves converting a numerical variable to a linguistic variable; five-sets triangular membership function are developed for the fuzzification as shown in Fig 4.



(a) Input Variable E (n), Fuzzification

(b) Input Variable CE (n), Fuzzification

(c) Output Variable (Imax), DeFuzzification

Fig. 4 FLC membership functions (a) the input variables e (n) (b) change of error ce (n) and (c) output variable defuzzification

Rule Elevator:

The basic fuzzy set operations needed for evaluation of fuzzy rules are $AND(\cap)$, $OR(\cup)$ and $NOT(-)$

AND -Intersection: $\mu_{A\cap B} = \min[\mu_A(X), \mu_B(x)]$

OR -Union: $\mu_{A\cup B} = \max[\mu_A(X), \mu_B(x)]$

NOT -Complement: $\mu_A = 1 - \mu_A(x)$

Defuzzification:

The rules of FLC generate required output in a linguistic variable format (Fuzzy Number), according to real world requirements, linguistic variables have to be transformed to crisp output (Real number).

Database:

The Database stores the definition of the membership function required by fuzzifier and defuzzifier

Rule Base:

The Rule base stores the linguistic control rules required

by rule evaluator, the 25-rules used in this paper are presented in table 1.

Table 1 Rule base table

e(n) / ce(n)	NM	NS	ZE	PS	PM
NM	NM	NM	NM	NS	ZE
NS	NM	NM	NS	ZE	PS
ZE	NM	NS	ZE	PS	PM
PS	NS	ZE	PS	PM	PM
PM	ZE	PS	PM	PM	PM

The desired reference source currents after compensation should be sinusoidal and it can be given as

$$i_{sa}^{*} = I_{\max} \sin \omega t \quad (8)$$

$$i_{sb}^{*} = I_{\max} \sin(\omega t - 120^{0}) \quad (9)$$

$$i_{sc}^{*} = I_{\max} \sin(\omega t + 120^{0}) \quad (10)$$

where $I_{\max}$ the amplitude of the desired source current and the phase angle can be obtained from the source voltages using unit sine vector. The reference currents $(i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*})$ are compared with actual source currents (i_{sa}, i_{sb}, i_{sc}) to generate switching signals for PWM-inverter using hysteresis current controller.

B) Hysteresis Band Current Control:

There are various current control methods proposed for APLC conFigurations; but in terms of faster current controllability and easy implementation, the hysteresis current control method scores over other current control techniques.

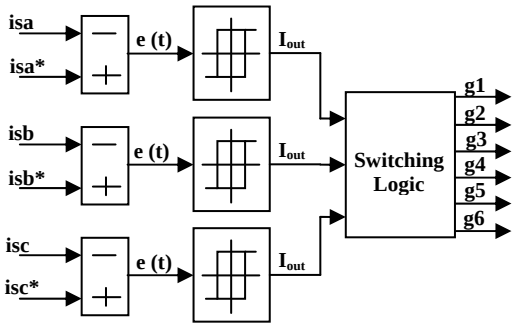


Fig 5 Structure of hysteresis current controller

Hysteresis band current control demonstrates characteristics like robustness, excellent dynamics and fastest control with minimum hardware. For the PWM-voltage source inverter; hysteresis current controllers are conFigured independently for each phase. Each current controller directly generates the switching signal of the three (a, b, c) phases shown in Fig 5. In the case of positive input current, if the error current $e(t)$ between the desired reference current $i_{ref}(t)$ and the actual source current $i_{actual}(t)$ exceeds the upper hysteresis band limit (*+h)*, the upper switch of the inverter arm is become OFF and the lower switch is become ON. As a result, the current starts to decrease. If the error current $e(t)$ crosses the lower limit of the hysteresis band (-h), the lower switch of the inverter arm is become OFF and the upper switch is become ON. As a result, the current gets back into the hysteresis band and the cycle repeats.

$$S = \begin{cases} 0 & if\ i_{actual}(t) > i_{ref}(t) + h \\ 1 & if\ i_{actual}(t) < i_{ref}(t) - h \end{cases} \quad (11)$$

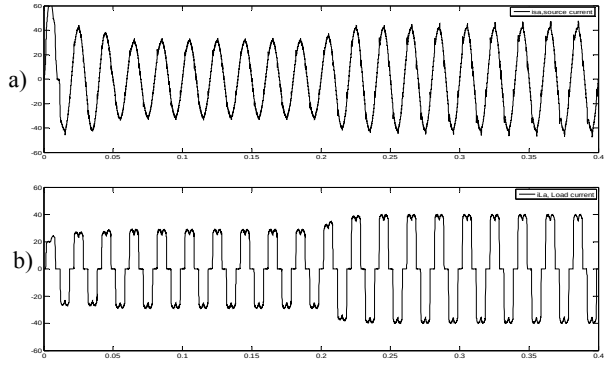
Here the hysteresis band limit used is h=0.5. The range of the error signal $e(t)$ directly controls the amount of ripple voltage in the output current from the PWM-VSI.

IV. Simulation Result and Analysis

The SIMULINK toolbox in the MATLAB is used to model and test the system under steady state and transient conditions using PI, Fuzzy logic and combination of PI and fuzzy logic controllers. The system parameter values are; source voltage (Vs) is 230 Vrms, System frequency (f) is 50 Hz, Source impedance R_S, L_S is 1 Ω; 0.2 mH respectively, Filter impedance R_c, L_c is 1 Ω; 2.5 mH, Load impedance R_L, L_L of diode rectifier RL load in steady state: 20 Ω; 200 mH and in transient: 10 Ω; 100 mH respectively, DC link capacitance (C_{DC}) is 1600μF, Reference Voltage (V_{DC}) is 400V and Power devices are IGBT with a freewheeling diode in anti parallel.

PI with Fuzzy controller:

PI with Fuzzy logic controller based APLC system comprises a three-phase source, a nonlinear load (six pulse diode rectifier RL load) and a PWM voltage source inverter with a dc capacitor on dc side. The simulation of the source current after compensation is presented in Fig. 6 (a) that indicates that the current becomes sinusoidal. The load current is shown in 6 (b). The actual reference current for phase is shown in Fig. 6(c). This wave is obtained from our proposed controller. The APLC supplies the compensating current that is shown in Fig. 6(d). The current after compensation is as shown in (a) which would have taken a shape as shown in (b) without APLC. It is clearly visible that this waveform is sinusoidal with some high frequency ripples. We have additionally achieved power factor correction as shown in Fig. 6(e), phase (a) voltage and current are in phase.



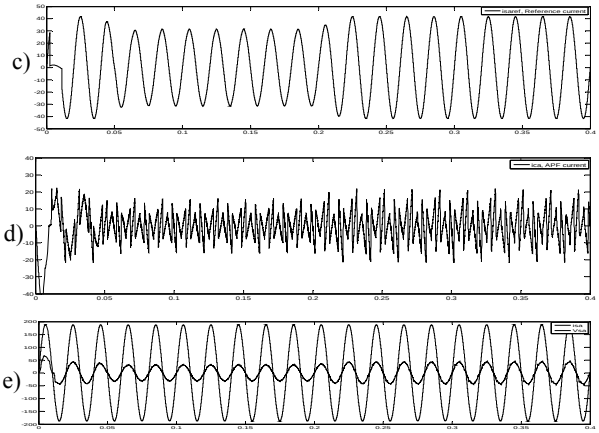


Fig. 6 PI with Fuzzy logic controller based simulation results for three-phase active-power-filter under the steady state condition (a) Source current after APLC, (b) Load currents, (c)Reference currents by the Fuzzy logic algorithm, (d) Compensation current by APLC and (e) unity power factor

First we conducted simulation (time T=0 to T=0.4s) with rectifier load with RL at output with values 20 ohms and 200 mH respectively and then RL load is suddenly changed to 10 ohms and 100 mH for transient condition. The transient simulation waveforms are plotted in a similar manner and are shown in Fig 7.

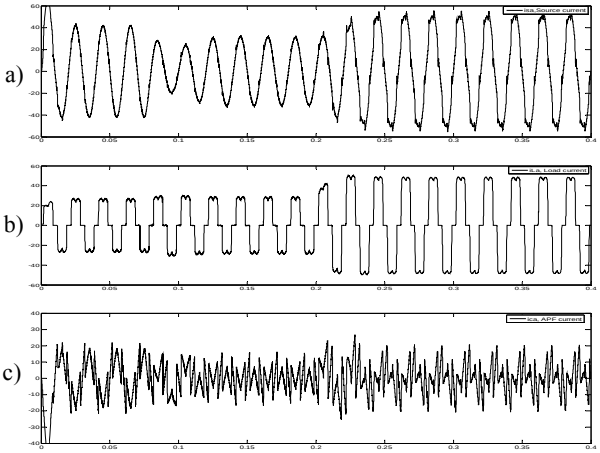
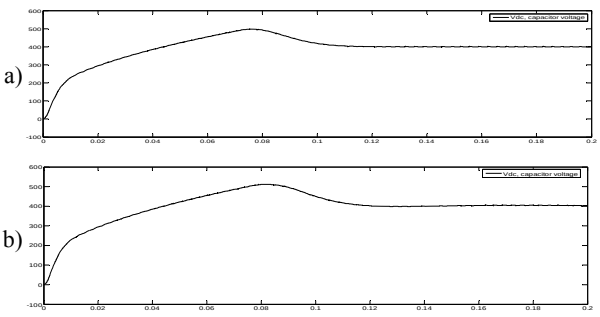


Fig. 7 PI with Fuzzy logic controller based simulation results for three-phase active-power-filter under the transient condition (a) Source current after APLC, (b) Load currents and (c) Compensation current by APLC

The DC side capacitor voltage is effectively controlled by the PI or FLC and/or combination of PI with FLC shown in Fig 8. It is observed that settling time is quite fast. The combination of PI with FLC takes least settling time and has small ripples compared to individual PI and FLC controllers.



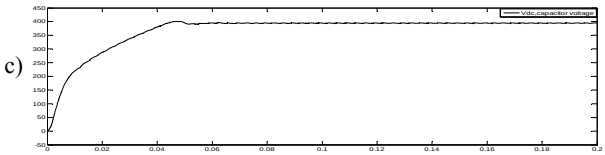


Fig. 8 simulation results for 3-phase APLC under steady state condition; waveform of DC side capacitor voltage controlled by (a) PI controller (b) FLC controller (c) PI with FLC controller

The dc-side capacitor voltage settling time in transient and steady state conditions using different controller are presented in table 2

Table 2 Vdc settling time using PI, FLC and PI with FLC controller

Condition	PI controller	Fuzzy controller	PI with Fuzzy Controller
Steady state	0.12s	0.11s	0.065s
Transient	0.13s	0.12s	0.060s

The PI with fuzzy logic controller based APLC system effectively suppresses the harmonics, compensates reactive power and improves power factor. Real power in watts (W) and reactive power in volt-amperes (VAR) are measured under steady state and transient condition and are presented in table 3

Table 3 Active and Reactive power measurement using PI, FLC and PI with FLC controller

Load Condition	Without APLC	Power measurement With APLC	
Steady state	P=3.907 kW Q=219 VAR	PI	P=4.039 kW Q=81 VAR
		Fuzzy	P=4.033 kW Q=72 VAR
		PI with Fuzzy	P=4.057 kW Q=75 VAR
Transient	P=4.847 kW Q=268 VAR	PI	P=4.97 kW Q=41 VAR
		Fuzzy	P=4.98 kW Q=40 VAR
		PI with Fuzzy	P=5.17 kW Q=36 VAR

The Fourier analysis of the source current is done to find magnitudes of different harmonic components and is shown in Fig 9.

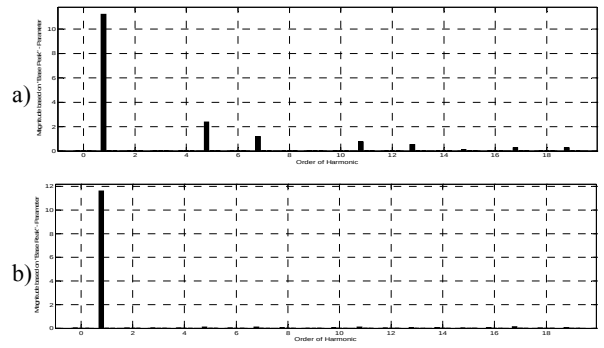


Fig. 9 PI with FLC-controller based harmonics measured with respect to the magnitude under the steady state condition (a) Source current without APLC, (b) source currents with active power line conditioners

The total harmonic distortion (THD) is computed. PI with FLC based shunt APLC indicates that THD of the source current is less than 5% after compensation that is in compliance with IEEE-519 standards harmonic, shown in table 4

Table 4 THD measurement using PI, FLC and PI with FLC controller

Load Condition	Without APLC	THD measurement With APLC		
		PI controller	Fuzzy controller	PI with Fuzzy logic Controller
Steady state	26.28%	3.10%	2.87%	2.52%
Transient	26.37%	3.18%	2.79%	2.32%

V. CONCLUSION

Proportional-Integral in conjunction with fuzzy logic controller based Shunt APLC performs quite well and it compensates both harmonic currents and reactive power. Simulation results demonstrate that source current after compensation is sinusoidal and is in phase with source voltage. PI with FLC facilitates reduction of ripples in dc-side capacitor of the inverter. The PI, FLC and PI with FLC-controllers are investigated under both steady state and transient conditions and it is observed that PI with FLC-controllers provides superior performance in terms of compensation and settling time compared to other methods. The PI with FLC based APLC system is in compliance with the IEEE-519 standards harmonics.

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BIOGRAPHIES

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Dynamic Performance Analysis of Self-commutating PWM CSI-fed Induction Motor Drive under MATLAB Environment

S. M. Tripathi [1] A. K. Pandey [2]

Abstract–In this paper, an attempt has been made to investigate analytically the dynamic performance of self-commutating current source inverter-fed induction motor drive with volts/Hz control strategy. Speed and current PI regulators are used in realization of closed loop control structure of the drive system. The closed loop mathematical modeling of the complete drive system is presented in the synchronously rotating d^e-q^e reference frame. The dynamic performance curves of the drive are obtained through MATLAB simulation and are discussed in detail.

Keywords–Current source inverter, induction motor drive, pulse width modulation (PWM), dynamic performance, V/f control.

NOMENCLATURE

d, q	Direct and quadrature axes
v_{as}, v_{bs}, v_{cs}	Phase voltages of the PWM inverter
v_{ds}^e	*d*-axis stator voltage in synchronously rotating reference frame
i_{ds}^e	*d*-axis stator current in synchronous rotating reference frame
v_{qs}^e	*q*-axis stator voltage in synchronously rotating reference frame
i_{qs}^e	*q*-axis stator current in synchronously rotating reference frame
i_{dr}^e	*d*-axis rotor current in synchronously rotating reference frame
i_{qr}^e	*q*-axis rotor current in synchronously rotating reference frame
i_{as}, i_{bs}, i_{cs}	Line currents of PWM inverter
I_{DC}	DC link current
I_{act}	Active component of stator current
I_{act}^*	Reference active component of stator current
I_{react}	Reactive component of stator current
I_{react}^*	Reference reactive component of stator current
ω_e	Switching frequency of the inverter
ω_r	Rotor speed of the induction motor
ω_{ref}	Reference speed
ω_{sl}	Slip speed of the induction motor
ω_{sl}^*	Reference slip speed
I_{ref}	Reference DC link current
V_{inv}	Input voltage of the inverter
V_r	Rectifier output voltage
R_f	Resistance of DC link inductor
L_f	Inductance of DC link inductor
R_s	Resistance of stator winding per phase
L_s	Self-inductance of stator winding per phase
R_r	Resistance of rotor winding per phase
L_r	Self inductance of rotor winding per phase
L_m	Mutual inductance per phase
L_1	$L_s L_r - L_m^2$
C	Capacitance per phase
J	Moment of inertia in kg-m2
B	Viscous friction coefficient
β	Pulse width of PWM rectifier
V_{LL}	Line-to-line input voltage of the rectifier
P	Number of poles
I_c	Instantaneous phase current of capacitor
V_s	Instantaneous stator phase voltage
i_{dc}^e	*d*-axis capacitor current in synchronously rotating reference frame
i_{qc}^e	*q*-axis capacitor current in synchronously rotating reference frame
k_{p_i}	Proportional gain of current regulator
k_{i_i}	Integral gain of current regulator
k_{p_s}	Proportional gain of speed regulator
k_{i_s}	Integral gain of speed regulator
p	Differential operator (d/dt) or complex frequency
k	$\frac{\text{Maximum value of fundamental inverter line current}}{\text{DC link current}}$
k_1	Slope of stator active current (I_{act}) *vs.* slip speed (ω_{sl})
k_2	Slope of stator reactive current vs. slip speed (ω_{sl})
k_{11}	$\frac{\text{Rated value of capacitor current per phase}}{[\text{Rated angular frequency } (\omega_e)]^2}$

I. INTRODUCTION

The speed control of induction motors is possible over a wide range by feeding the motor through variable frequency VSI or CSI. Due to the controlled current operation of the inverter, slip-regulated CSI is preferred over VSI. The current source at the front end makes the system naturally capable of power regeneration [1]–[4]. In this paper, the closed loop scheme of self-commutating current source inverter-fed induction motor drive employing two PI regulators is presented. The selection of parameters for current and speed PI regulators of a self-commutating CSI-fed induction motor drive are made on the basis of system relative stability, frequency scanning, and transient response of the drive, as thoroughly discussed in [5].

II. SYSTEM DESCRIPTION

The CSI-fed induction motor drive consists of a three-phase AC source, a PWM rectifier, a DC link smoothening reactor, a current-controlled inverter, a three-phase squirrel cage induction motor, and a three-phase capacitor bank, as shown in Figure 1. A fast-response speed-

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regulating drive can be realized by incorporating PI regulators in the feedback loops [6]–[9]. Two PI regulators are used – one in the speed feedback loop and the other in the current feedback loop. The outer speed regulator compares the reference speed and the actual rotor speed and processes the speed error to obtain the reference slip speed (ω_{sl}^*) which is required to estimate the reference stator active current (I_{act}^*) and reference stator reactive current (I_{react}^*) of the induction motor and hence, reference DC link current (I_{ref}). It is also used in the calculation of switching frequency (ω_e) of the inverter. The following mathematical equations are used:

$$\omega_{sl}^* = \left(k_{p_s} + \frac{k_{i_s}}{p} \right) (\omega_{ref} - \omega_r) \tag{1}$$

$$I_{act}^* = k_1 \, \omega_{sl}^* + \text{constant} \tag{2}$$

$$I_{react}^* = k_2 \, \omega_{sl}^* + \text{constant} \tag{3}$$

$$\omega_e = \omega_r + \omega_{sl}^* \tag{4}$$

The current PI regulator is used to regulate the error between the reference DC link current and actual DC link current. The output of current PI regulator decides the pulse widths of the PWM rectifier pulses and hence, controls the output voltage of the pulse width modulated rectifier, which in turn controls the DC link current. The output voltage of the rectifier in terms of current regulator parameters is given by the following expression:

$$V_r = \left(k_{p_i} + \frac{k_{i_i}}{p} \right) (I_{ref} - I_{DC}) \tag{5}$$

The reference DC link current is determined using the equation:

$$I_{ref} = \left(\sqrt{\left(I_{act}^*\right)^2 + \left(I_{react}^* - I_{c'}\right)^2} \right) . \left(\frac{\sqrt{2}}{k} \right) \tag{6}$$

For the V/f control operation of the drive I_c may be expressed as

$$I_c = k_{11} \, \omega_e^{\,2} \tag{7}$$

where, $k_{11} = \dfrac{I_{c\,(rated)}}{(\omega_{e\,(rated)})^2}$

III. Mathematical Model of the Drive

The modeling of the PWM CSI-fed induction motor drive is carried out in synchronously rotating reference frame for the following:

A. Three-phase PWM rectifier
B. Three-phase PWM inverter
C. DC link
D. Three-phase induction motor with load
E. Three-phase capacitor bank

A. Three-phase PWM rectifier

The PWM rectifier output voltage depends on the number of pulses per cycle and their widths. The converter is modeled for twelve numbers of equal pulses per cycle. It leads to two pulses per 60° each of β width. The average output voltage of the PWM rectifier can be expressed as follows:

$$V_r = \frac{3\sqrt{2}}{\pi} V_{LL} \left(4 \sin \frac{5\pi}{12} \right) \sin \frac{\beta}{2} \tag{8}$$

Since β is varied from 10% to 90% of (π/6) radians, hence, (β/2) is very small and it can be approximated as follows: sin (β/2) ≅ (β/2). Therefore,

$$V_r = 5.218 \, V_{LL} \, (\beta / 2) \tag{9}$$

B. Three-phase PWM inverter

The fundamental component of the line currents of the three-phase pulse width modulated inverter i_{as}, i_{bs}, and i_{cs} forms a balanced set of three-phase currents with maximum value as $I_{as(max)}$ and can be expressed as follows:

$$I_{as\,(\max)} = k I_{DC} \tag{10}$$

where, k is obtained through Fourier analysis of inverter line current waveforms, and this is given by the following:

$$k = \frac{\text{maximum value of fundamental inverter line current}}{\text{DC link current } (I_{DC})}$$

The value of k depends on the operating frequency of the inverter and varies from 0.8485 to 0.9970 for variation in operating frequencies from 10 to 50 Hz. Since the inverter output fundamental current peak is taken along the q^e axis of the reference frame, the transformed phase current equations in the d^e-q^e reference frame are as follows:

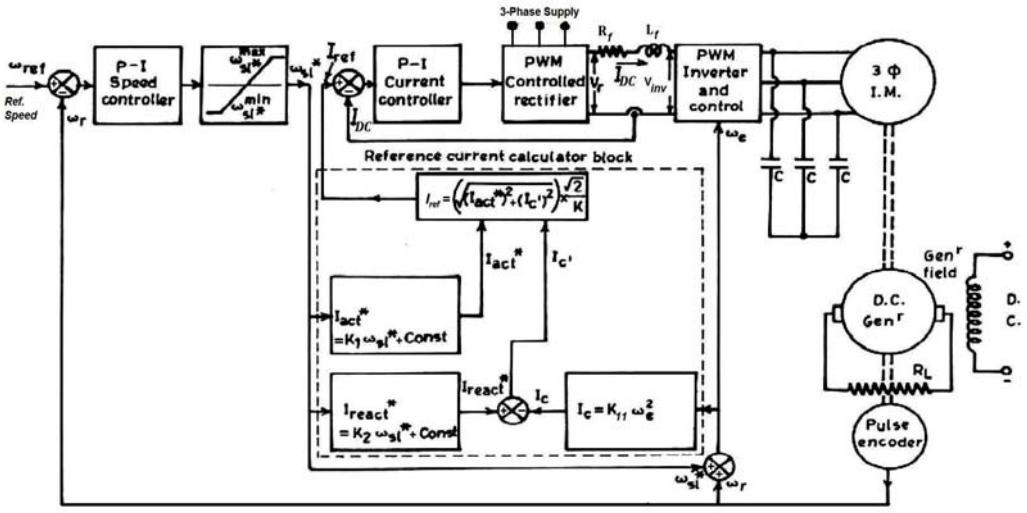

Fig. 1: Variable speed self-commutating PWM current source inverter fed induction motor drive

$$i_{0s}{}^{e} = 0 \;;\; i_{qs}{}^{e} = kI_{DC} \;;\; i_{ds}{}^{e} = 0 \tag{11}$$

Assuming power loss in the inverter to be negligible, *i.e.*, input power = output power, we can derive the following:

$$V_{inv}I_{inv} = v_{as}i_{as} + v_{bs}i_{bs} + v_{cs}i_{cs} = \frac{3}{2}\left(v_{qs}{}^{e}i_{qs}{}^{e} + v_{ds}{}^{e}i_{ds}{}^{e}\right) \tag{12}$$

Substituting the values of $i_{qs}{}^{e}$, $i_{ds}{}^{e}$, and I_{inv} in terms of I_{DC}, the following equation is obtained:

$$V_{inv} = 1.5\,k\,v_{qs}{}^{e} \tag{13}$$

C. DC link

The rectifier output voltage V_r is the sum of the inverter input voltage V_{inv} and DC link voltage, hence

$$V_r = 1.5\,k\,V_{qs}{}^{e} + \left(R_f + pL_f\right)I_{DC} \tag{14}$$

D. Three-phase induction motor with load

The induction motor can be modeled in the d^e-q^e reference frame using the following assumptions:

- The three-phase stator windings of the motor are balanced and sinusoidally distributed in space.
- The air gap flux is maintained at rated value.
- The motor line currents are sinusoidal due to capacitor at the motor terminals.
- The DC link current is ripple free.
- The inverter switching transients are ignored.
- There is no core loss in the motor.

The motor can be described by fourth-order matrix equation in d^e-q^e reference frame as follows:

$$\begin{bmatrix} v_{qs}^{e} \\ v_{ds}^{e} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s + pL_s & \omega_e L_s & pL_m & \omega_e L_m \\ -\omega_e L_s & R_s + pL_s & -\omega_e L_m & pL_m \\ pL_m & \omega_{sl} L_m & R_r + pL_r & \omega_{sl} L_r \\ -\omega_{sl} L_m & pL_m & -\omega_{sl} L_r & R_r + pL_r \end{bmatrix} \begin{bmatrix} i_{qs}^{e} \\ i_{ds}^{e} \\ i_{qr}^{e} \\ i_{dr}^{e} \end{bmatrix} \tag{15}$$

The electromagnetic torque equation of the motor is expressed as follows:

$$T_e = \frac{3}{2}.\frac{P}{2}.L_m\left(i_{qs}{}^{e}i_{dr}{}^{e} - i_{qr}{}^{e}i_{ds}{}^{e}\right) \tag{16}$$

The equation of motion of the drive is given by the following:

$$T_e = T_l + J\frac{d\omega_r}{dt} + B\omega_r \tag{17}$$

The load torque equation is expressed as

$$T_l = T_L.\left(\omega_r/\omega_{base}\right) \tag{18}$$

E. Three-phase capacitor bank

The capacitor current is related to the stator voltage of the induction motor, as shown below:

$$i_c = C\frac{dv_s}{dt} \tag{19}$$

Transforming (19) in the synchronously rotating reference frame d^e-q^e, we have the following:

$$\left(i_{dc}^{e}\cos\omega_e t - i_{qc}^{e}\sin\omega_e t\right) = C\frac{d}{dt}\left(v_{ds}^{e}\cos\omega_e t - v_{qs}^{e}\sin\omega_e t\right) \tag{20}$$

Differentiating (20) and comparing the terms on both sides, *d*-axis and *q*-axis currents are expressed as follows:

$$i_{dc}^{e} = C\left(pv_{ds}^{e} - \omega_e v_{qs}^{e}\right) \tag{21}$$

$$i_{qc}^{e} = C\left(pv_{qs}^{e} + \omega_e v_{ds}^{e}\right) \tag{22}$$

IV. Dynamic Performance Analysis

A three-phase capacitor bank of 150 µF per phase is preferred at the motor terminals for the near sinusoidal current over a wide range of operating frequency [6]. The dynamic performance of the drive is investigated through MATLAB simulation by implementing the designed values of regulator parameters and using the mathematical model of the drive along with analyzing the current and speed transient responses of the drive for the following cases:

1. Start-up
2. Decrease in load torque
3. Increase in load torque
4. Speed deceleration
5. Speed acceleration
6. Speed acceleration and decrease in load torque
7. Speed deceleration and increase in load torque
8. Speed deceleration and decrease in load torque
9. Speed acceleration and increase in load torque
10. Speed reversal

The current and speed responses of the drive employing aforesaid transient conditions one by one each after an interval of 10 seconds are shown in Figure 2. However, the dynamic performance of the drive can be analyzed well by considering the speed and current responses of the drive separately for each transient condition as depicted in Figures 3-4.

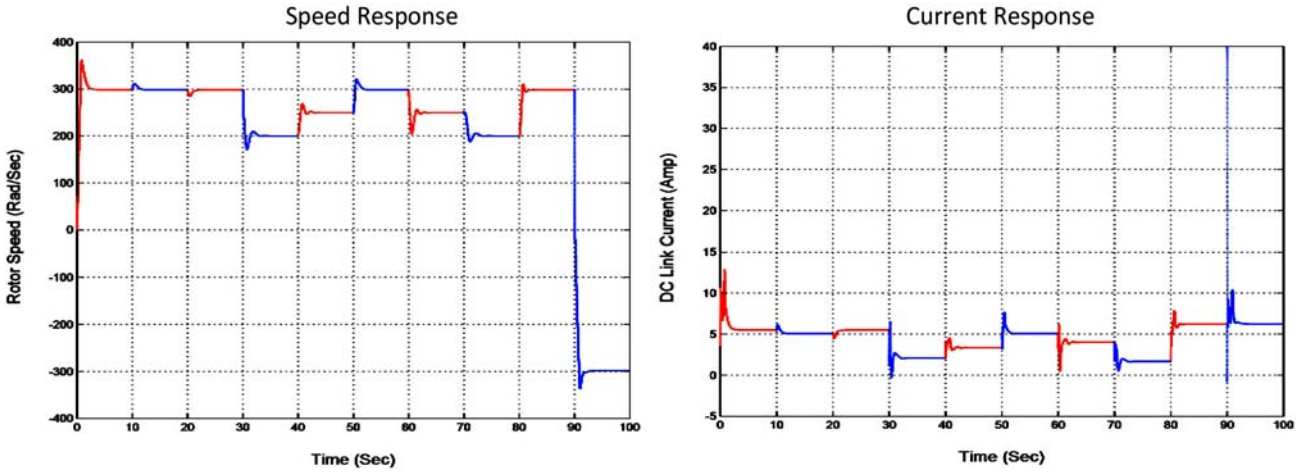

Fig. 2: Speed and current responses of the drive employing different transient conditions each after an interval of 10 seconds.

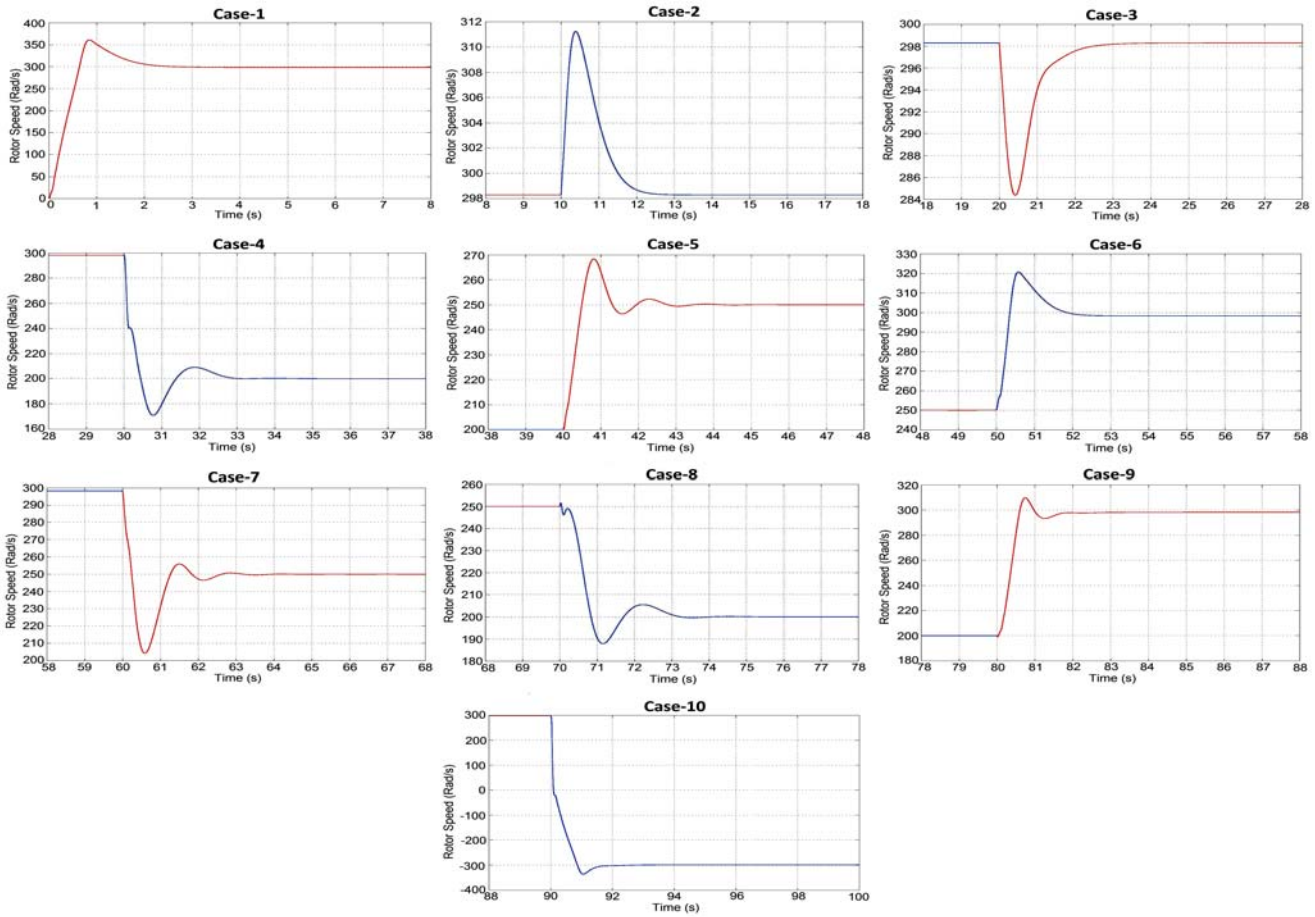

Fig. 3: Speed responses of the drive separately for each transient case.

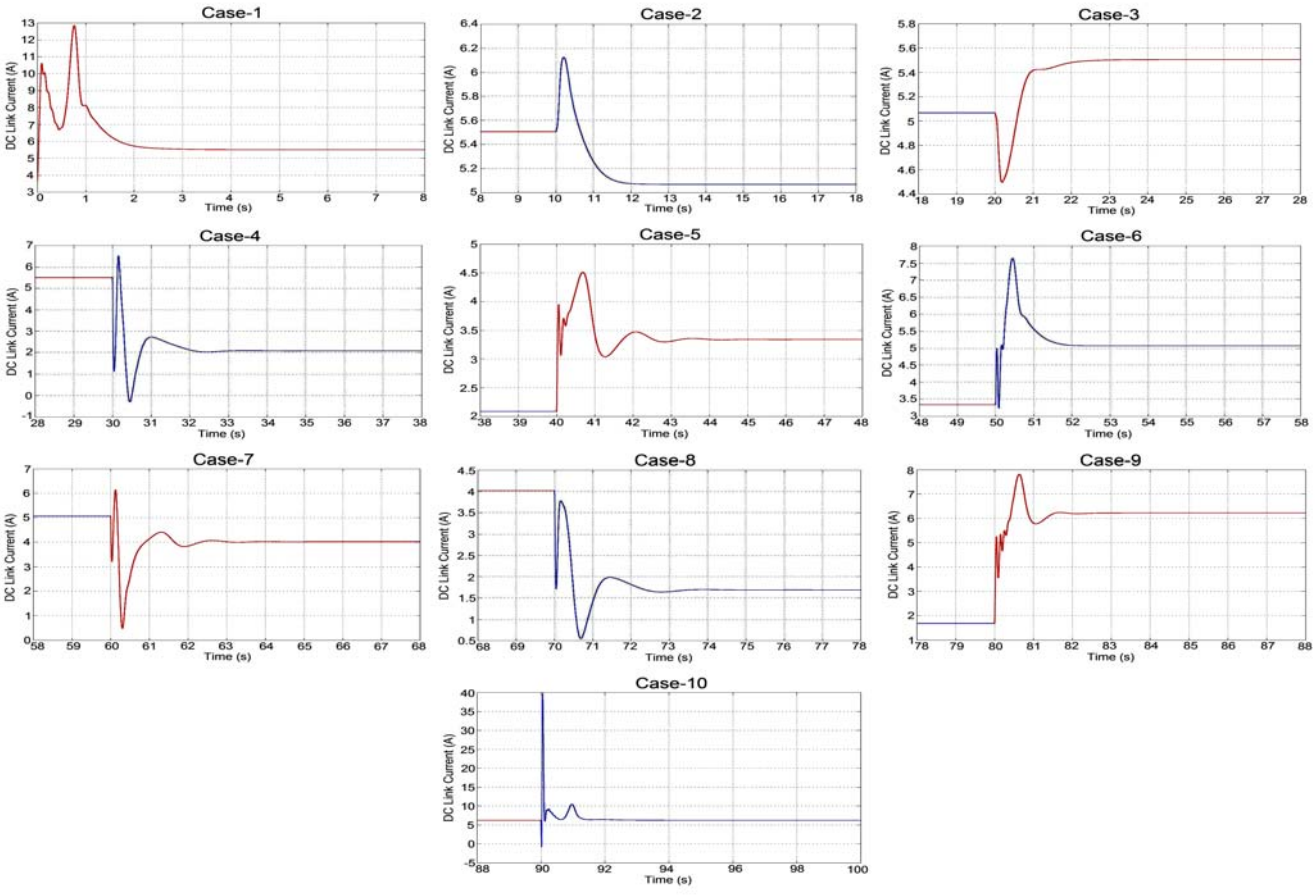

Fig. 4: Current responses of the drive separately for each transient case.

Case–1: Start-up

Initially the motor is at stand still. A step speed command of rated value (298.29 rad/s) from standstill is furnished. Speed PI regulator sets the speed of the rotor at the reference speed selected without exceeding the permissible over shoot limit of the speed in 3.24 seconds as depicted in Figure 3 (case-1). The DC link current corresponding to rotor speed (298.29 rad/s) and load torque (1.31 N-m) is realized 5.506 A as shown in Figure 4 (case-1).

Case–2: Decrease in load torque

The load torque on the motor running at 298.29 rad/s is reduced to 1.00 N-m immediately after 10 seconds and as a result the rotor speed tends to increase but it again settles to 298.29 rad/s in 3.19 seconds as depicted in Figure 3 (case-2). The steady-state value of the DC link current corresponding to rotor speed (298.29 rad/s) and load torque (1.00 N-m) decreases to 5.068 A as shown in Figure 4 (case-2).

Case–3: Increase in load torque

The load torque on the motor running at 298.29 rad/s is now increased to 1.31 N-m immediately after 20 seconds and as a result the rotor speed tends to decrease but it again settles to 298.29 rad/s in 3.21 seconds as shown in Figure 3 (case-3).
It can be observed from Figure 4 (case-3) that the DC link current corresponding to rotor speed (298.29 rad/s) and load torque (1.31 N-m) acquires the same steady-state value (5.506 A) as in the case-1.

Case–4: Speed deceleration

The reference speed of the motor running at 298.29 rad/s is changed to 200 rad/s immediately after 30 seconds and the motor in turn starts decelerating and settles to 200 rad/s in 3.17 sec. as shown in Figure 3 (case-4). The steady-state value of the DC link current corresponding to rotor speed (200 rad/s) and load torque (1.31 N-m) decreases to 2.087 A as depicted in Figure 4 (case-4).

Case–5: Speed acceleration

The reference speed of the motor running at 200 rad/s is changed to 250 rad/s immediately after 40 seconds and the motor in turn starts accelerating and settles to 250 rad/s in 3.69 seconds as shown in Figure 3 (case-5).
The steady-state value of the DC link current corresponding to rotor speed (250 rad/s) and load torque (1.31 N-m) increases to 3.340 A as depicted in Figure 4 (case-5).

Case–6: Speed acceleration and decrease in load torque

The reference speed of the motor running at 250 rad/s is changed to 298.29 rad/s and the load torque on the motor is decreased to 1.00 N-m together immediately after 50 seconds and as a result the rotor speed starts accelerating and it settles to 298.29 rad/s in 2.87 seconds as depicted in Figure 3 (case-6).
It can be observed from Figure 4 (case-6) that the DC link current corresponding to rotor speed (298.29 rad/s) and load torque (1.00 N-m) acquires the same steady-state value (5.068 A) as in the case–2.

Case–7: Speed deceleration and increase in load torque

The reference speed of the motor running at 298.29 rad/s is changed to 250 rad/s and the load torque on the motor is increased to 1.85 N-m together immediately after 60 seconds and as a result the rotor speed starts decelerating and it settles to 250 rad/s in 3.65 seconds as depicted in Figure 3 (case-7). It can be observed from Figure 4 (case-7) that the steady-state value of the DC link current corresponding to rotor speed (250 rad/s) and load torque (1.85 N-m) decreases to 4.023 A, though this value is higher than the steady-state value of case–5 on account of increased load torque.

Case–8: Speed deceleration and decrease in load torque

The reference speed of the motor running at 250 rad/s is changed to 200 rad/s and the load torque on the motor is decreased to 1.00 N-m together immediately after 70 seconds and as a result the rotor speed starts decelerating with an early swing and it settles to 200 rad/s in 3.43 seconds as depicted in Figure 3 (case-8). It can be observed from Figure 4 (case-8) that the DC link current corresponding to rotor speed (200 rad/s) and load torque (1.00 N-m) decreases to 1.689 A, which is lower than the steady-state value of case–4 on account of decreased load torque.

Case–9: Speed acceleration and increase in load torque

The reference speed of the motor running at 200 rad/s is changed to 298.29 rad/s and the load torque on the motor is increased to 1.85 N-m together immediately after 80 seconds and as a result the rotor speed starts accelerating with a relatively tiny early swing and it settles to 298.29 rad/s in 3.02 seconds as depicted in Figure 3 (case-9). It can be observed from Figure 4 (case-9) that the DC link current corresponding to rotor speed (298.29 rad/s) and load torque (1.85 N-m) increases to 6.230 A, which is the highest among the steady-state values of the cases – 1, 2, 3 and 6 on account of very high load torque.

Case–10: Speed reversal

Figure 3 (case-10) shows the response of the motor drive to the reversal of speed. The motor is running stably at positive set reference speed of rated value (298.29 rad/s) and immediately after 90 seconds the set speed is changed to -298.29 rad/s. In response to this change, the speed regulator is actuated and the drive system control structure implements the braking at controlled frequencies followed by its reverse motoring up to the set reference speed in 3.84 seconds. It can be seen from Figure 4 (case-10) that the DC link current corresponding to rotor speed (-298.29 rad/s) and load torque (1.85 N-m) attains the previous steady-state value (6.230 A).

As summarized in Table-1, the DC link current and drive settling time corresponding to different transient conditions stated aforesaid, it is found that the steady-state value of the DC link current is increased / decreased with increase / decrease in motor speed and / or in load torque. The speed PI regulator maintains the speed to its set reference value for variation in the load torque within the prescribed limit. The speed settling takes place in the time duration 2.87-3.84 seconds. The dynamic performance

curves and facts in Table-1 show the effectiveness of speed and current PI regulators.

Table-1: Summary of different cases

Case	Step-change in Reference Speed (rad/s)		Step-change in Load Torque (N-m)		DC Link Current (A)	Drive Settling Time (s)
	From	To	From	To		
1	0	298.29	1.31		5.506	3.24
2	298.29		1.31	1.00	5.068	3.19
3	298.29		1.00	1.31	5.506	3.21
4	298.29	200	1.31		2.087	3.17
5	200	250	1.31		3.340	3.69
6	250	298.29	1.31	1.00	5.068	2.87
7	298.29	250	1.00	1.85	4.023	3.65
8	250	200	1.85	1.00	1.689	3.43
9	200	298.29	1.00	1.85	6.230	3.02
10	298.29	-298.29	1.85		6.230	3.84

V. CONCLUSIONS

A closed-loop scheme incorporating speed and current PI regulators of the V/Hz controlled PWM self-commutating CSI-fed induction motor drive has been discussed. A mathematical model of the induction motor drive has been developed by considering different sections of the model to investigate the dynamic performance of the drive system. The exploration of the dynamic response curves obtained through MATLAB simulation has confirmed that the control structure of the drive takes care of transients in a proper time. It is also observed that the level of the transient current never exceeds the permissible value. Therefore, it is concluded that the motor control scheme takes care of the over current of the inverter devices. The proposed scheme has confirmed that there are quick and instantaneous changes in the DC link currents in accordance with any disturbances in the reference speed / load torque thereby provides fast response of the drive system.

APPENDIX

Name plate ratings of induction motor

1 hp, three-phase, 400 V, 50 Hz, 4-pole, 1425 rpm, star

Induction motor parameters

R_s = 3.520 Ω R_r = 2.780 Ω L_s = 0.165 H
L_r = 0.165 H L_m = 0.150 H J = 0.01289 kg-m^2

DC link parameters

R_f = 0.250 Ω, L_f = 0.040 H

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BIOGRAPHIES

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Voltage Sag Restorer with Diode-Clamped Multilevel Bridge

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Abstract—Voltage sag restorer is developed using a multi-level diode clamped inverter with a number of series-connected bulk capacitor for different voltage level. Although the multilevel circuit has more component count than the two-level circuit it is more suitable for high voltage applications. The restorer is bypassed under normal operating conditions and is connected to the load depending upon voltage sag detection. The switches of the inverter are controlled by PWM signals. In the paper the operation of the multilevel circuit is simulated in SABER to study the operating capability of the multilevel inverter. A comparative study between the traditional two-level circuit and the proposed multilevel circuit is provided to highlight the performance of the multilevel circuit. The proposed topology is designed, tested and confirmed by experimental results. The proposed circuit can eliminate the conventional problem of filter and the dynamic performance is excellent. Overall performance of the circuit is satisfactory.

Index Terms—Voltage sag, Power interruption, Power system, Diode-Clamped, Multilevel

I. INTRODUCTION

The reliability for the recent years for the power distribution has been significantly improved to prevent the power interruption by power electronic converter systems [1, 2]. Besides the electromagnetic interference and harmonics, the voltage sags are also the most common power disturbance and power quality problems [2-14]. The voltage sags are caused by faults on adjacent lines or starting of motors. This is getting more important nowadays because of the sensitivity of the high speed computer controlled equipment. The non-zero impedance of a power grid causes voltage drop at the point where the load is connected. Usually, these drops are very small such that the voltage remains within normal ranges [15]. But under heavy load condition where there is a large increase in current, or when the impedance of the system is high, a significant voltage drop may occur. Such voltage variations are not desirable for sensitive loads[8, 16]. Voltage sags are defined as a decrease in root mean square (rms) voltage at the power frequency. Voltage sag is not a complete interruption of power but a momentary drop in the magnitude of the voltage. It is a temporary drop below 90 percent of the nominal voltage level. Most voltage sags do not go below 50 percent of the nominal voltage, and they normally last from 3 to 10 cycles—or 50 to 170 milliseconds[3]. Sags do not generally disturb incandescent or fluorescent lighting, motors, or heaters.

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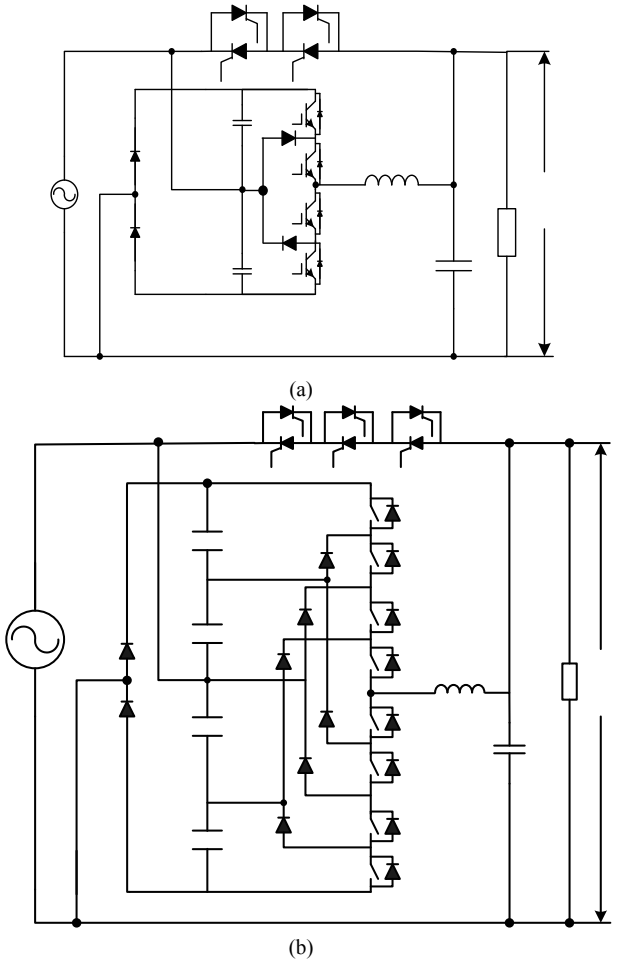

Fig. 1. Single-phase voltage sag restorer with multilevel diode-clamped bridge (a) Three-level (b) Five-level circuit

However, some electronic equipment lacks sufficient internal energy storage and, therefore, cannot ride through sags in the supply voltage [15].

Power conversion solution has been used recently to mitigate sags. They are for examples designing inverter drives for process equipment to be more tolerant of voltage fluctuations or the installation of voltage correction devices. Survey has found that the installation of voltage sag restorer is a better solution rather than to develop a high performance front-end converter for each sensitive equipment. The device is also called a dynamic voltage restorer (DVR) [17]. DVR is one of the custom power devices capable of protecting sensitive loads from all supply-side disturbances. Numerous circuit topologies and methods are available for DVR[2, 5, 6, 8-11, 13, 17-36]. DVR is different from uninterruptable power supply because UPS ahs to handled the full power for the sensitive equipment, whereas DVR is only to handle the reduced power from the nominal value. Therefore it is more cost effect and usually is higher dynamic performance. It also only needs to operate

when needed rather than like the UPS which is needed to online all the times. The main limitation of some of the solutions is the use of 50 Hz interfacing transformer. As a result the power electronics circuits are limited in application by presence of low frequency transformer, which must be able to handle full rated power[37]. In order to address this issue, dynamic voltage sag correctors(DySC) without an interfacing transformer are proposed[32, 37, 38]. The topology is derived from a voltage boost circuit and is small in size and weight. The standard DySC products, up to 500-kVA modules, do not include a series transformer, and include little energy storage. The topology is also different from the single inverter with transformer that is used properly in wind power generation [39] For high voltage application, the switches with high voltage rating have to be used in such circuits. In this paper, a single-phase voltage sag restorer with multilevel diode-clamped bridge is proposed by which the circuit can be used at high voltage but with switches of low voltage rating. Subharmonic PWM modulation method used for multilevel converters is employed for controlling the power switches in the circuit. Simulation results are provided to validate the feasibility of the proposed concept.

The diode-clamped multilevel bridge inverter circuit is discussed in II, operation of the voltage sag restorer is presented in III, and simulation results are given in IV followed by experimental results and conclusions.

II. Diode-Clamped Multilevel Bridge

A. Diode-Clamped multilevel converter

The schematic of a single phase Diode-clamped multilevel converter is shown in Fig. 2. In general, the output voltage of a given multilevel converter can be calculated from (1) as:

$$V_o = (S - \frac{n-1}{2})E \qquad (1)$$

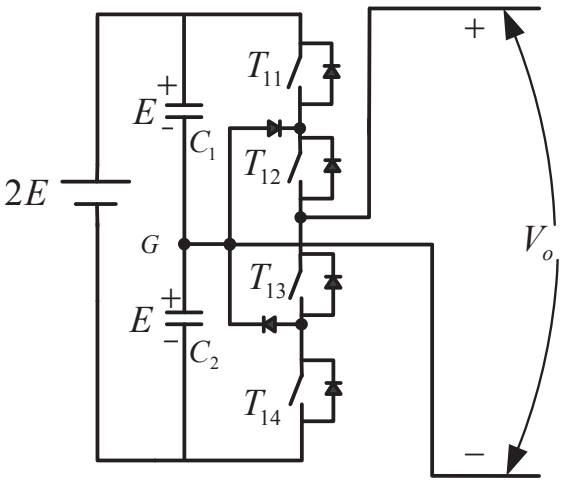

Fig. 2 Diode-clamp multilevel bridge

where V_0 is the output voltage of the multilevel converter, n is the number of the output levels; S is the switching state that ranges from 0 to n-1. E is the minimum voltage level the multilevel converter can generate.

Assuming the DC bus voltage of the converter is 2E, it can be easily found from Fig. 2, that when T_{11} ,T_{12} are on T_{13} ,T_{14} are off or T_{12} ,T_{13} are on T_{11} ,T_{11} and T_{14} are off or T_{11} ,T_{12} off T_{13},T_{14} on, the output voltage of V_o is +E, 0, -E, respectively. So the "S" ranges from 0, 1, 2 and three voltage levels can be synthesized.

B. Subhamonic PWM method

Subhamonic PWM is a conventional control method suitable for multilevel converter. The control principle of the SHPWM method is to compare several triangular carrier signals with only one sinusoidal reference signal per phase. For example, in an n-level inverter, n-1 triangular carrier signals of the same frequency f_c and the same peak-to peak amplitude A_c, are disposed such that the bands they occupy are contiguous.

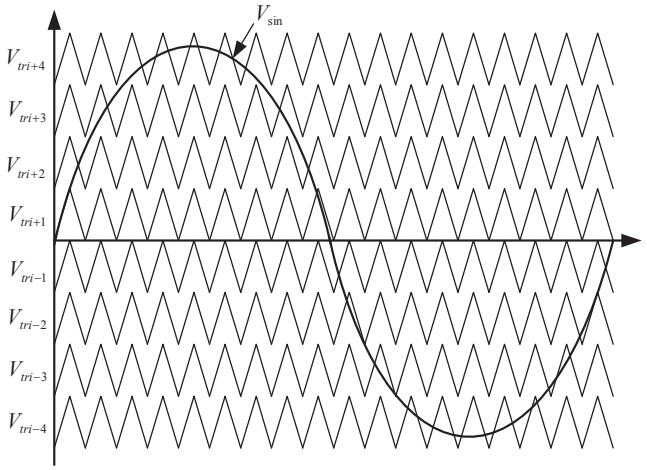

Fig. 3 Principle of Subhamonic PWM method.

The zero reference is placed in the middle of the carrier set. The modulation wave is a sinusoid of frequency f_m and amplitude A_m. At every instant, each carrier is compared with the modulation waveform generating the gating signal for the switches in the respective levels. Comparison of the respective triangular signals with the sine signal results in switching on of the devices if the reference signal is greater than the triangular carrier assigned to that device level; otherwise, the device is turned off. For example, in a nine-level inverter shown in Fig. 4, eight triangular carriers are compared with a sinusoid modulation waveform as shown in Fig. 3.

Whenever $V_{sin}>V_{tri+4}$ the switching state S is 8 resulting in an output voltage of V_{ac} equal to +4E， and whenever $V_{tri+4}>V_{sin}>V_{tri+3,}$ the switching state S is 7 resulting inV_{ac} equal to +3E and so on. On the other hand when $V_{sin}<V_{tri-4,}$ the switching state S is 0 and the output voltage V_{ac} is -4E. Thus different switching combination can be selected according to the switching state "S" to generate different voltage levels. The pattern generation is simple and can be easily to be implemented.

III. VOLTAGE SAG RESTORER WITH MULTILEVEL DIODE-CLAMPED BRIDGE

The voltage sag restorer proposed here is similar to the conventional voltage sag restorer but for the use of multilevel half-bridge diode-clamped inverter. As shown in Fig. 1, the single phase voltage sag restorer is derived from voltage doubler [20, 32, 33, 37, 38] and a half-bridge multilevel diode-clamped inverter. The inverter is configurable to work in voltage boost or bypass mode, and is capable of providing 100% step-up to the ac grid voltage. Under normal working conditions, the anti-parallel SCRs are closed, and a normal line voltage is provided directly from the input line. When any voltage sag is detected, the SCRs are opened and the multilevel inverter bridge is controlled to resurrect the voltage to the load.

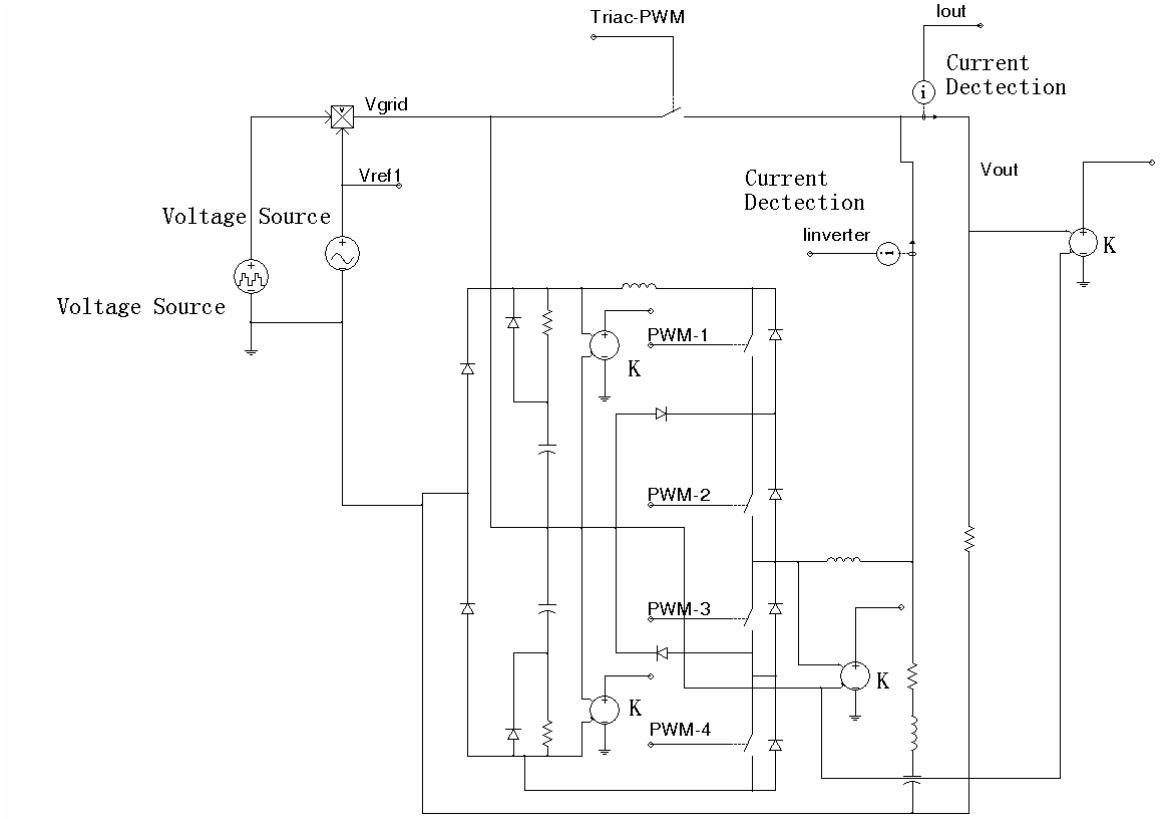

Fig. 4: Schematic of the main circuit of the proposed system

IV. SIMULATION VERIFICATION

The proposed DVR system based on three-level diode-clamped inverter bridge is simulated using the mixed-mode circuit simulation SABER program for a 2kVA load to verify the effectiveness of the proposed technique. A simulation model of the system shown in Fig. 1(a) is carried out. The schematic of the model is shown in Fig. 4 and the control circuit is shown in Fig.5. The voltage sag detection is implemented in the RMS voltage detection block as in Fig. 6.

The main parameters used in the simulation are given as: C_1= C_2=4700□F, L_s=5mH C_s=10□F and the switching frequency f_s is 10 kHz. Fig. 7 illustrates the voltage restoration performances of the three levels DVR system during source-side single-phase voltage sag. For duration of voltage sag of 0.25s, and the voltage is dipped from 310V to 180V, the output voltage is able to be maintained at constant 300V peak. There is a little transient of less than 3% of voltage transient, but the overall performance is highly satisfactory. Measured three-level PWM output voltage and inverter output are shown in Fig. 8. The measured driving signals and DC-link capacitor voltage are shown in Fig. 9 and Fig. 10 respectively.

It can be seen that there are voltage decrease gradually due to the voltage sag, and it returns to 310V at t=0.5s. Each capacitor voltage in the multi-level will also experience such variation abnd the prospoed converter can also compensate for the voltage sag and provide constant output voltage.

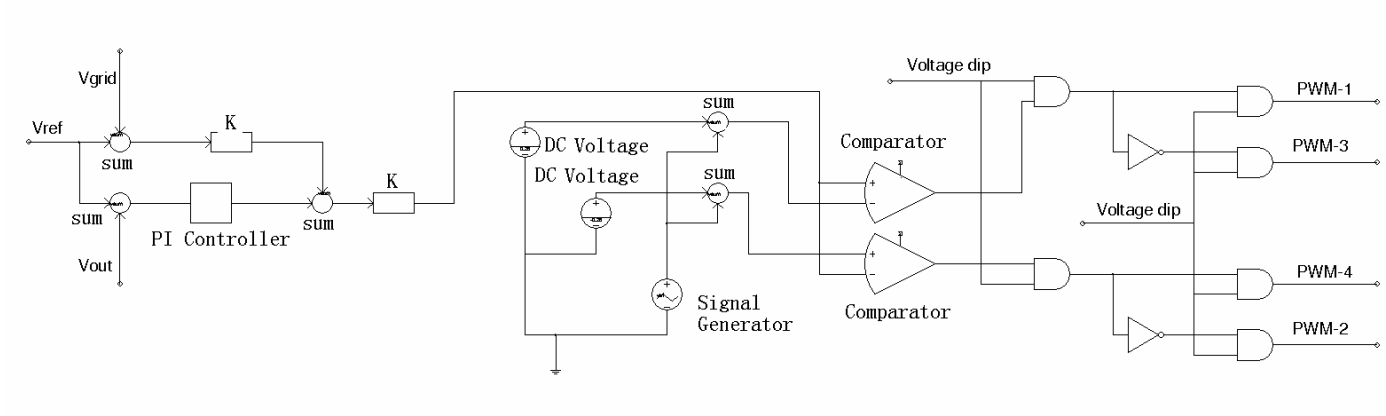

Fig. 5: Schematic of the control circuit of the proposed system

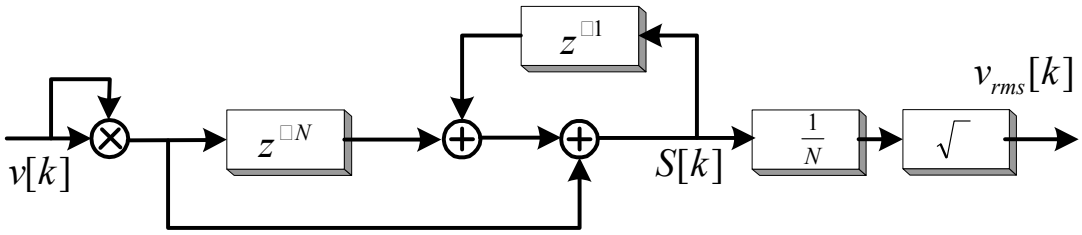

Fig 6: RMS voltage detection block

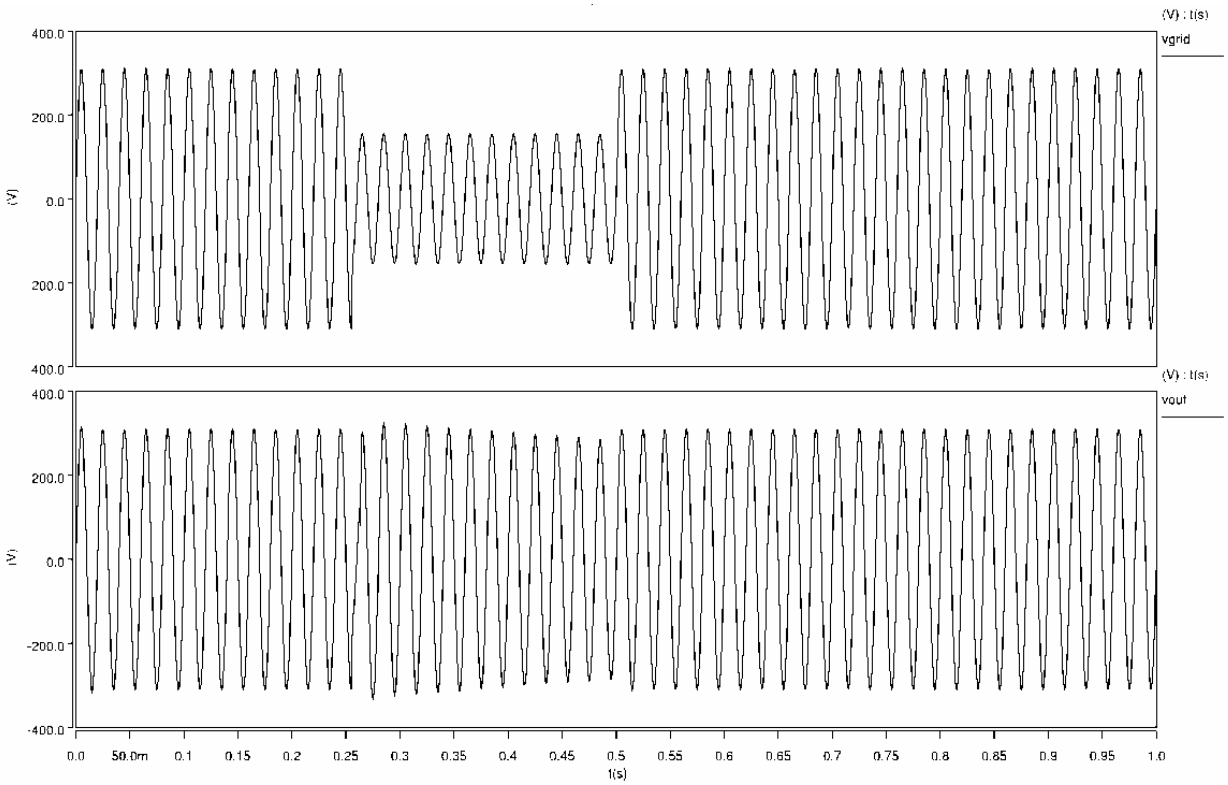

Fig. 7: Measured source-side single-phase voltage and the output voltage across load (2kVA).
Upper: source-side single-phase voltage, vgrid; Lower: output voltage, vout.

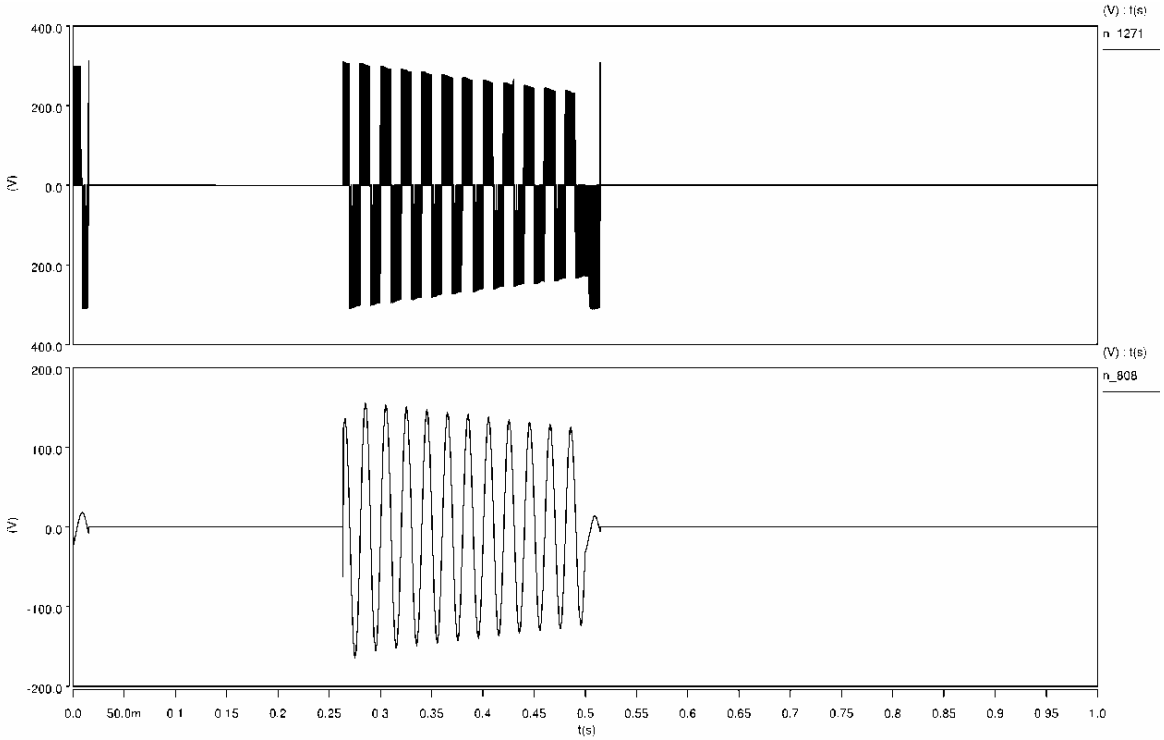

Fig. 8: Measured three-level PWM voltage and inverter output voltage
Upper: inverter three-level PWM voltage; Lower: inverter output voltage

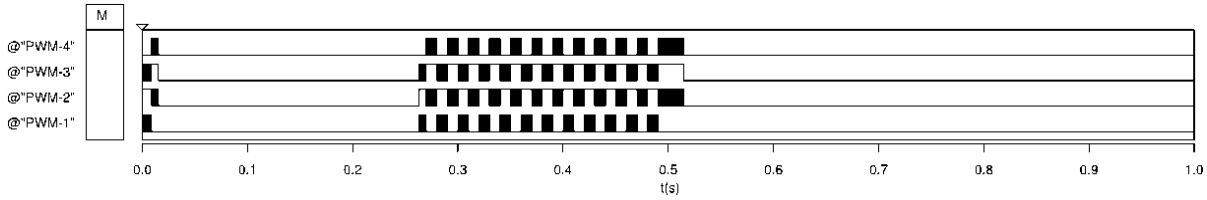

Fig. 9: Measured gate driving signals of switches in diode-clamped inverter bridge, PWM1~PWM4

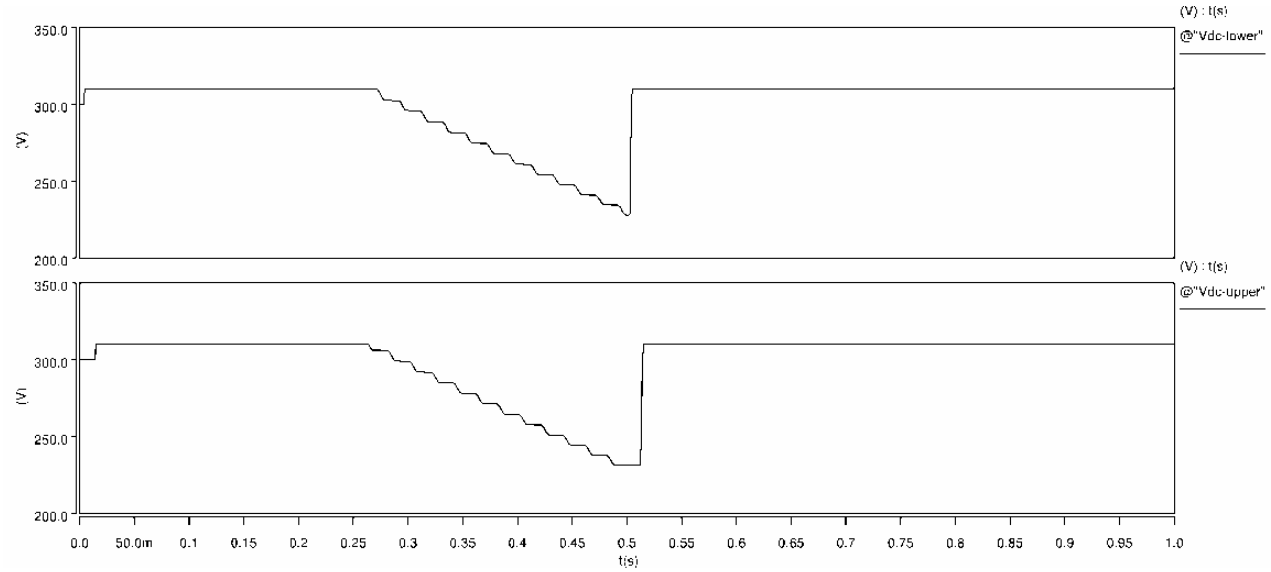

Fig. 10: Measured DC-link capacitor voltage
Upper: DC voltage across lower capacitor; lower: DC voltage across upper capacitor

V. Experimental Validation

A multilevel diode-clamped inverter based DVR system is developed in the Lab. The experimental result is given in Fig. 11. The input voltage drops to 50% of the nominal voltage with the sag duration of 500ms. The output voltage is not affected by the voltage sag during the sag duration as shown in CH 1.

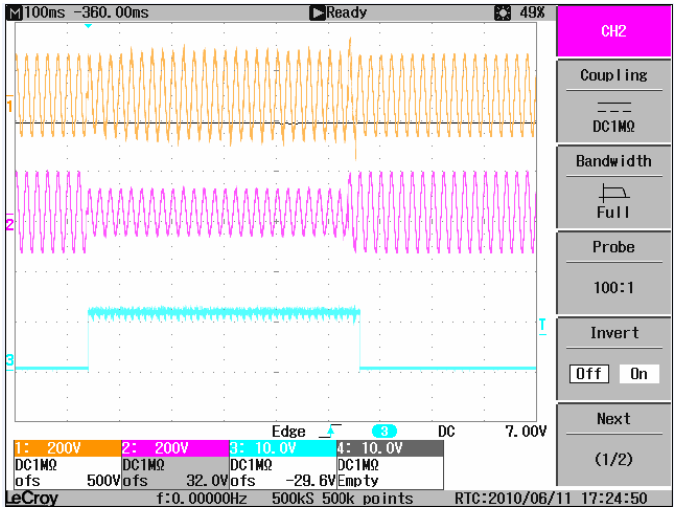

Fig .11: 1-Phase, 50%, 25cycle voltage Sag, 50Hz,
CH1: Output Voltage, 400V/Div, CH2: Input Voltage, 400V/Div,
CH3: Voltage Sag Signal, 10V/Div, Time Base: 100ms/Div

VI. Conclusion

A multilevel diode-clamped inverter based DVR system is proposed in this work. The circuit is derived from the multi-level concept for the inverter and is applied to the voltage sag compensation. In the circuit, the dc-bus voltage is split into several levels by series-connected bulk capacitors with neutral at the mid point. The advantages of the proposed topology when compared with two-level topology are: 1) Voltage stress across IGBT is reduced by half; 2) it can result in higher voltage levels; 3) Resulting in smaller size filter due to reduced harmonic content; 4) Suitable for high voltage application with lower rating switches such as for 10kV power transmission line. The disadvantages of the proposed topology are: 1) Higher component count; 2) Complicated control and large package layout. Also, the proposed topology is designed, simulated, tested and is used to verify the proposed circuit. Both simulation and experimental results are confirmed the successful operation of the proposed circuit.

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